FIG. 1A

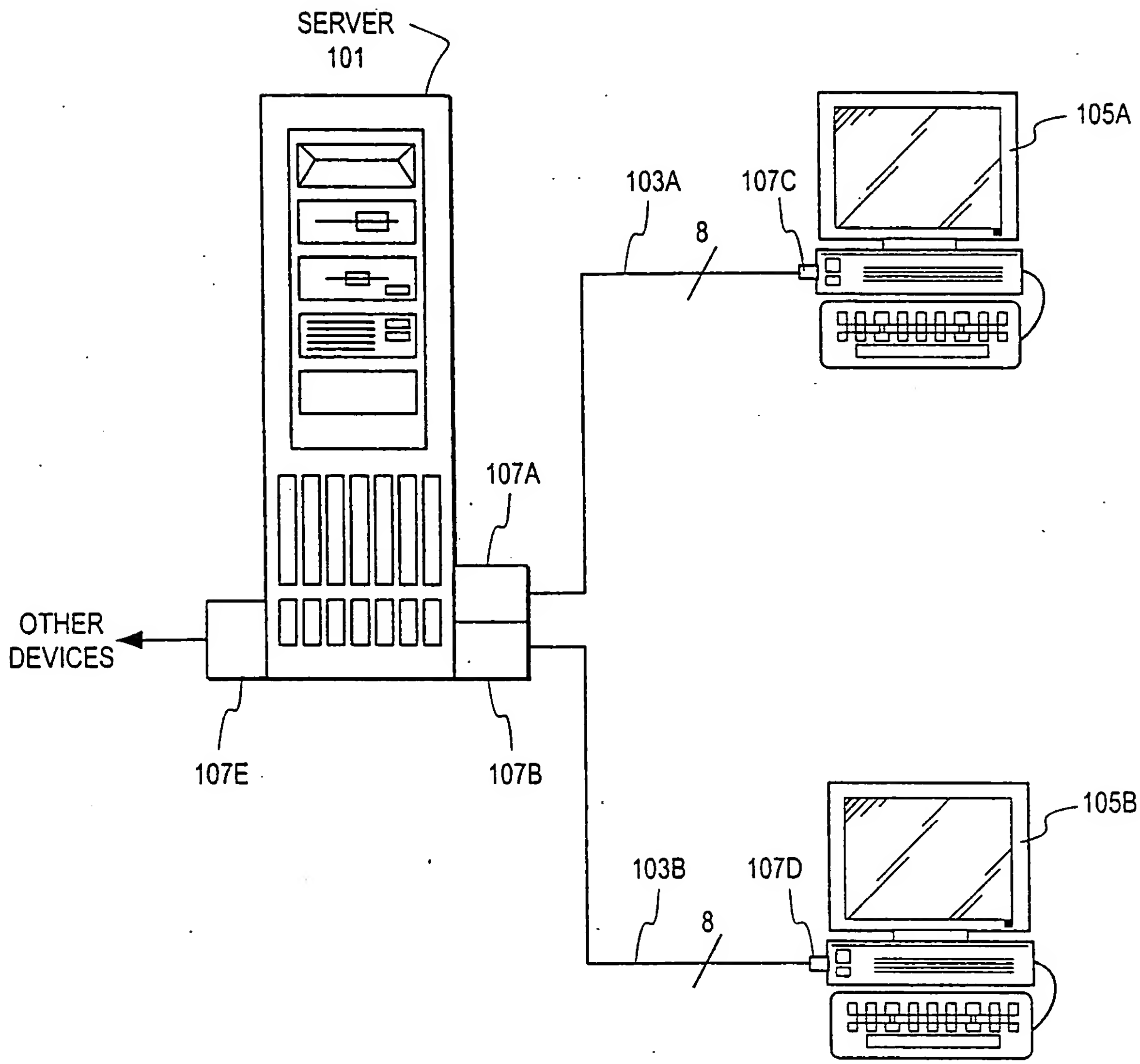
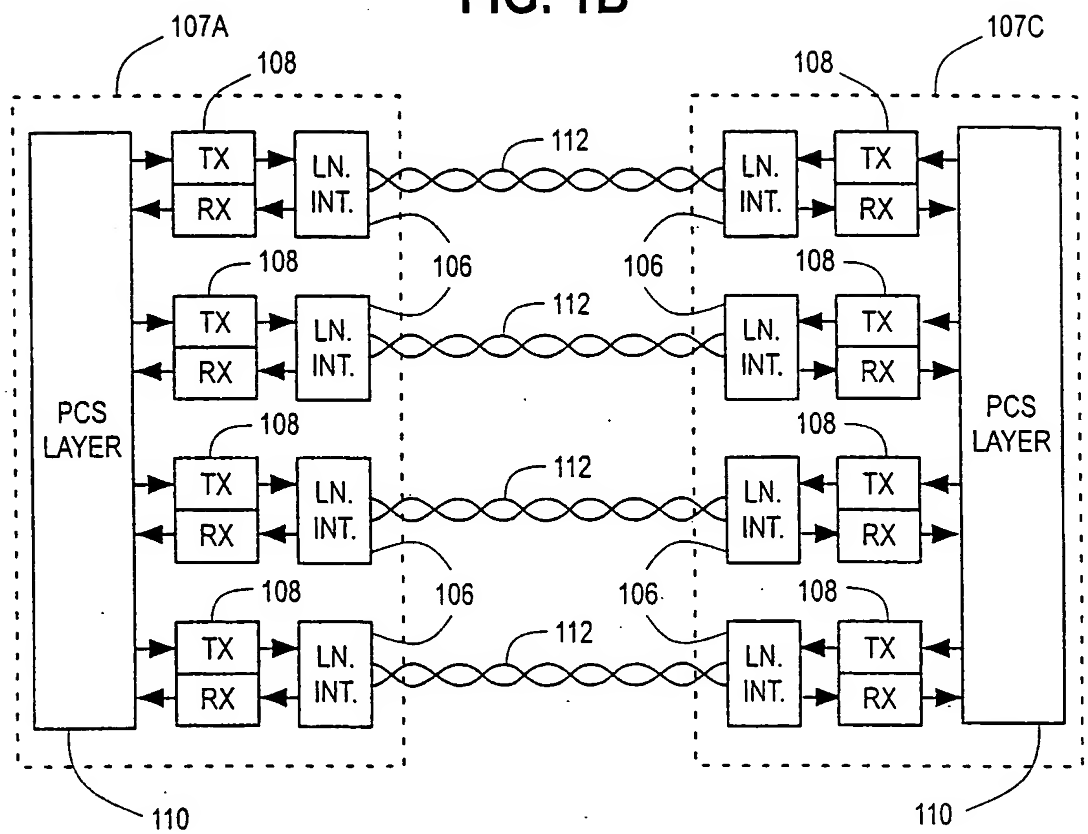

SERVER
101
105A
103A
107C
8
107A
OTHER
DEVICES
107E
107B
105B
103B
107D
8

FIG. 1B



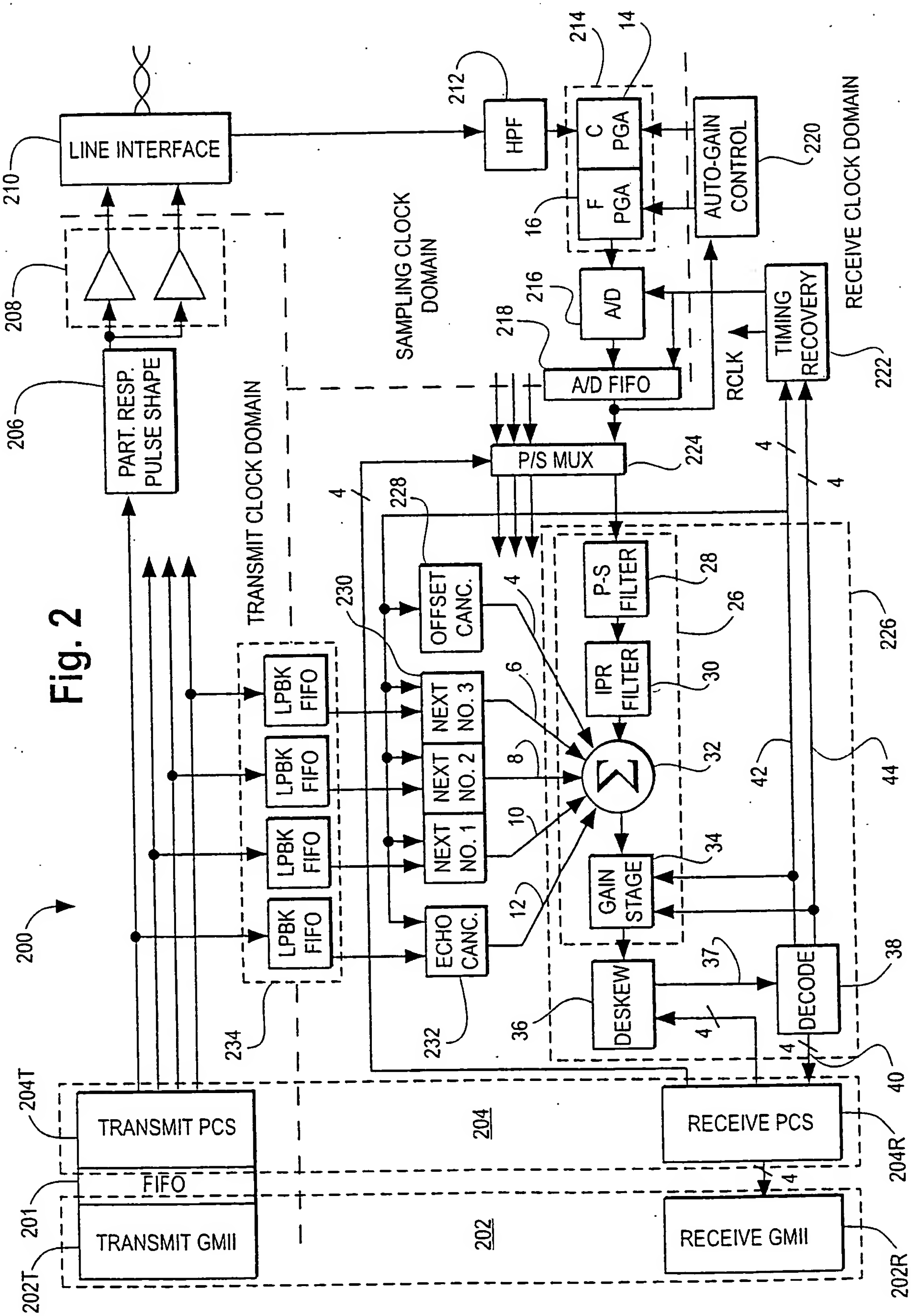

200
LINE INTERFACE
210
208
206
PART. RESP. PULSE SHAPE
TRANSMIT CLOCK DOMAIN
SAMPLING CLOCK DOMAIN
RECEIVE CLOCK DOMAIN
HPF
212
214
14
C PGA
F PGA
16
AUTO-GAIN CONTROL
220
A/D
216
A/D FIFO
218
TIMING RECOVERY
222
RCLK
P/S MUX
224
228
OFFSET CANC.
230
NEXT NO. 3
NEXT NO. 2
NEXT NO. 1
ECHO CANC.
232
LPBK FIFO
234
P-S FILTER
28
IPR FILTER
30
26
226
32
GAIN STAGE
34
DESKEW
36
DECODE
37
38
40
42
44
4
6
8
10
12
TRANSMIT PCS
204T
FIFO
201
TRANSMIT GMII
202T
204
202
RECEIVE PCS
204R
RECEIVE GMII
202R

Fig. 2

FIG. 3

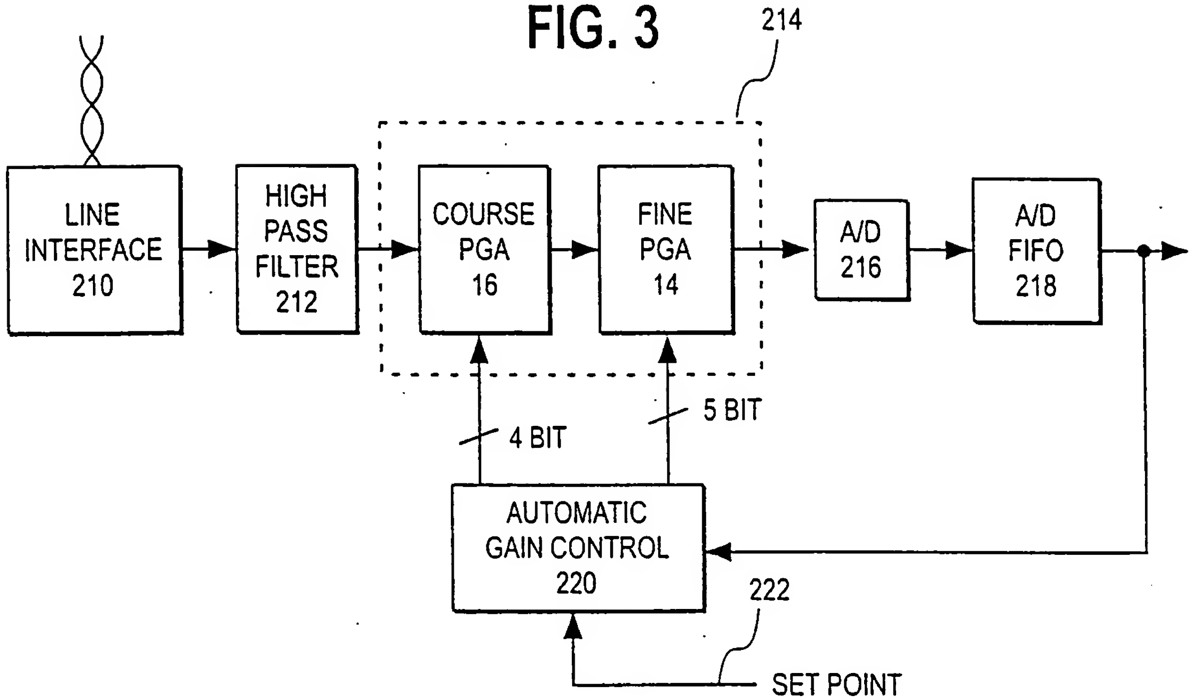

214
LINE INTERFACE 210
HIGH PASS FILTER 212
COURSE PGA 16
FINE PGA 14
A/D 216
A/D FIFO 218
4 BIT
5 BIT
AUTOMATIC GAIN CONTROL 220
222
SET POINT

FIG. 4

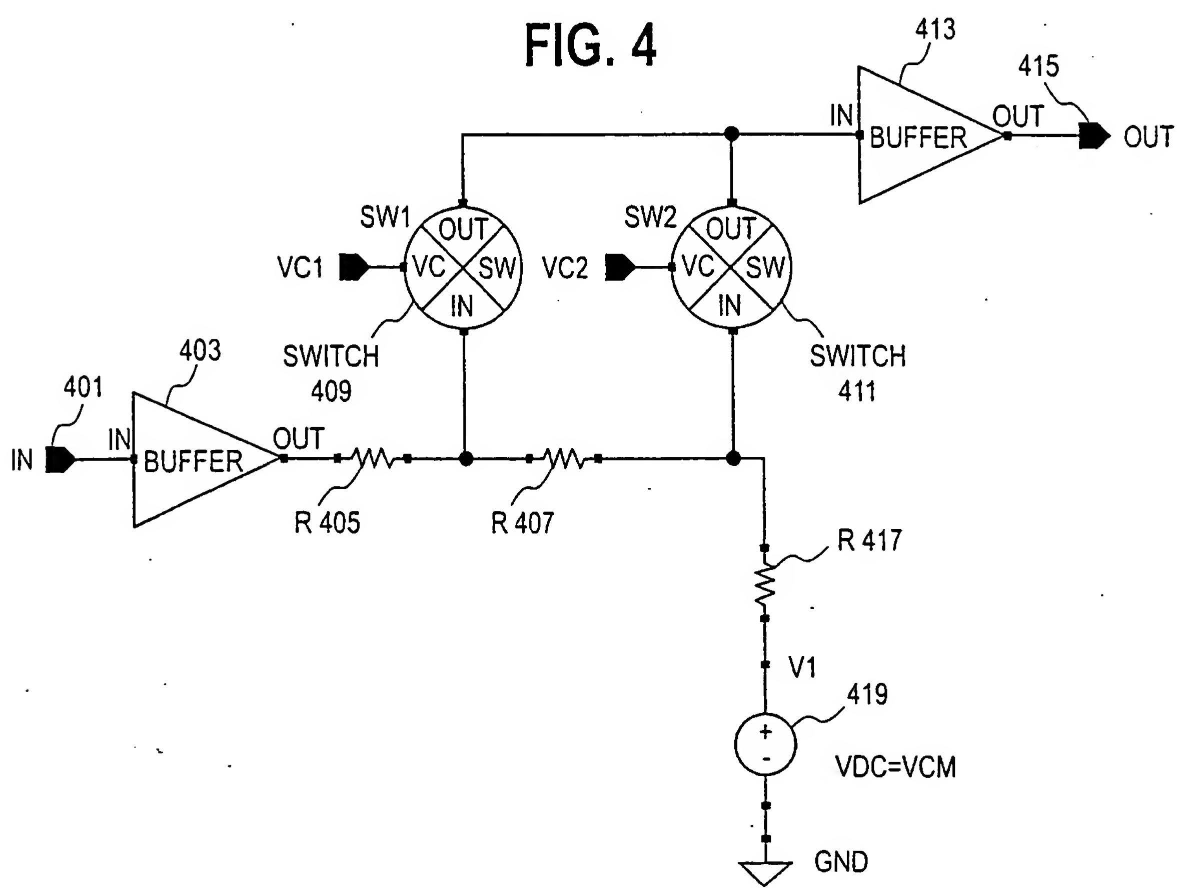

413
415
IN
BUFFER
OUT
OUT
SW1
OUT
VC
SW
IN
VC1
SWITCH 409
SW2
VC2
SWITCH 411
403
401
IN
BUFFER
R 405
R 407
R 417
V1
419
VDC=VCM
GND

FIG. 5

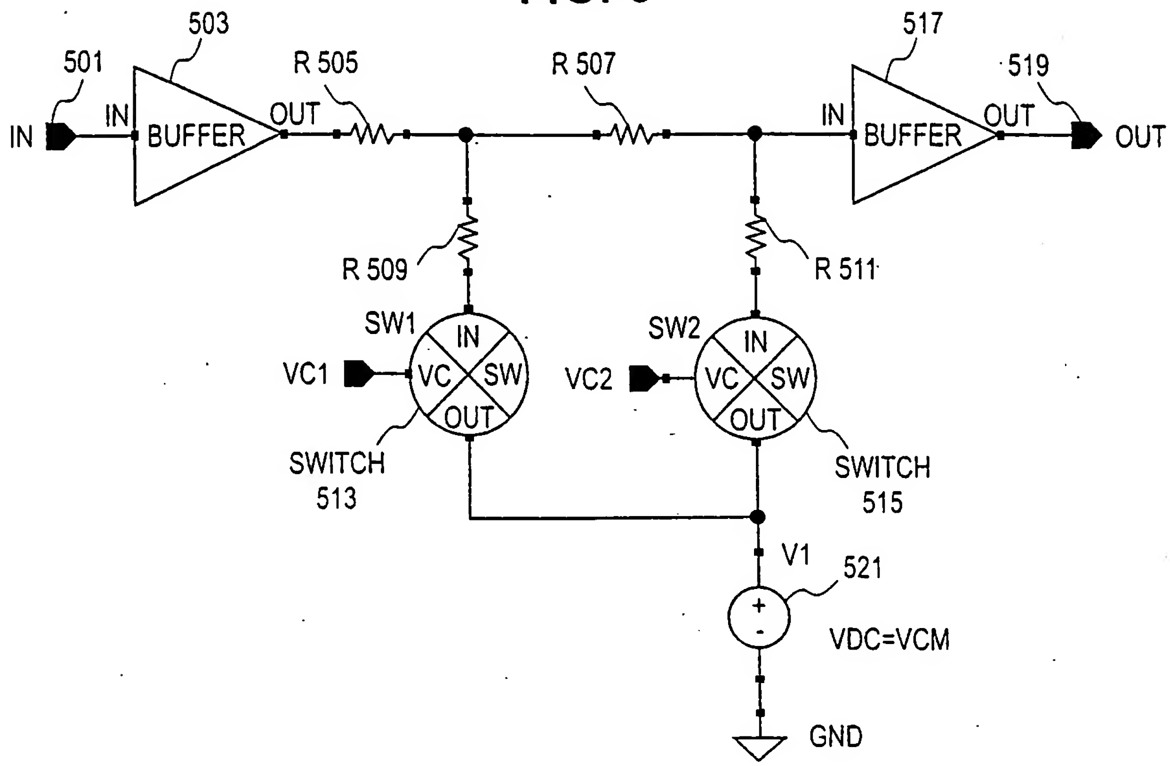
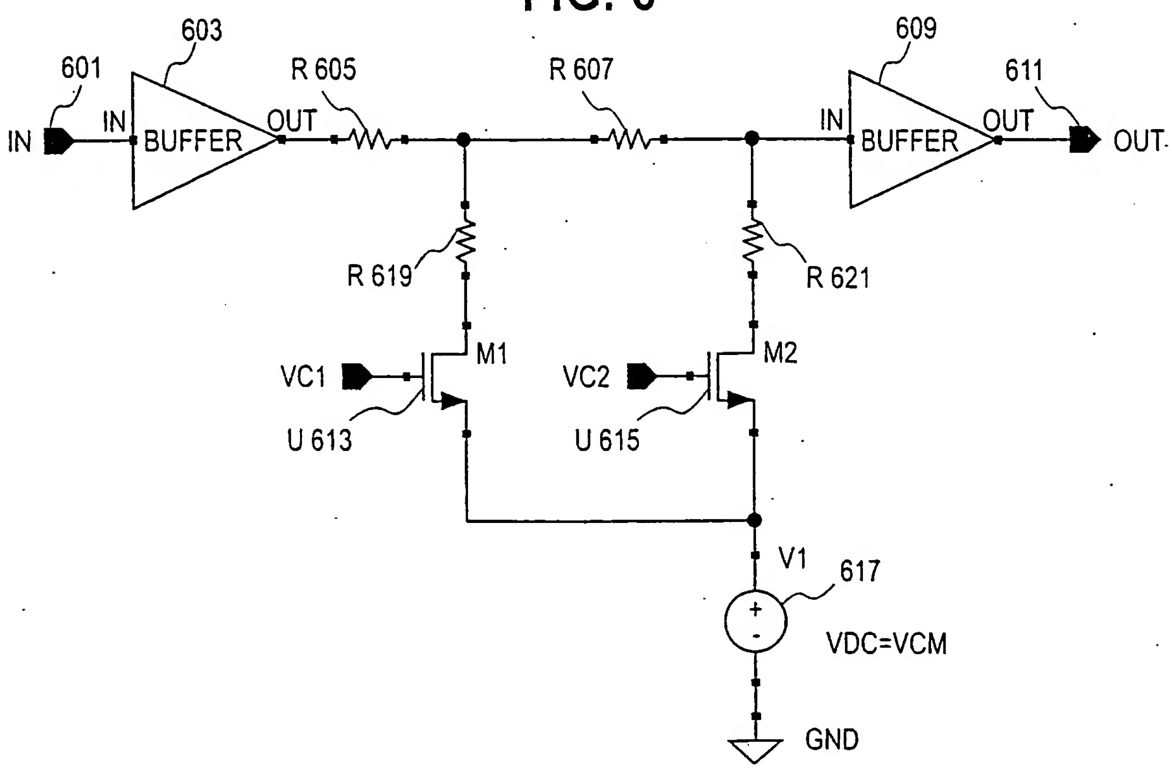

503
501
R 505
R 507
517
519
IN
IN
BUFFER
OUT
IN
BUFFER
OUT
OUT
R 509
R 511
SW1
IN
VC1
VC
SW
OUT
SWITCH
513
SW2
IN
VC2
VC
SW
OUT
SWITCH
515
V1
521
+
-
VDC=VCM
GND

FIG. 6


603
601
R 605
R 607
609
611
IN
IN
BUFFER
OUT
IN
BUFFER
OUT
OUT
R 619
R 621
M1
VC1
U 613
M2
VC2
U 615
V1
617
+
-
VDC=VCM
GND

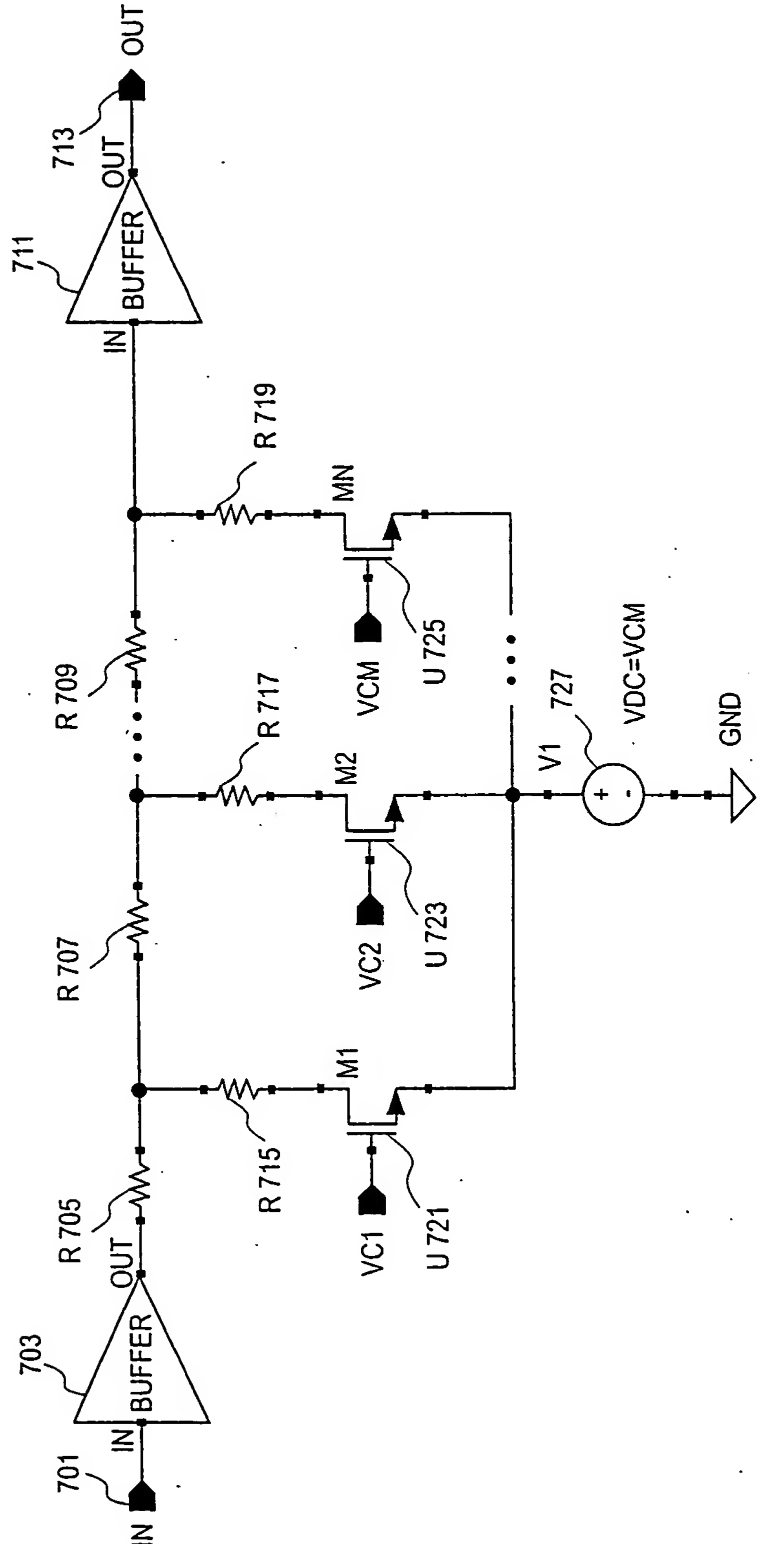

IN
701
IN
BUFFER
703
OUT
R 705
R 715
VC1
U 721
M1
R 707
VC2
U 723
M2
R 717
R 709
VCM
U 725
MN
R 719
IN
BUFFER
711
OUT
713
OUT
V1
727
VDC=VCM
GND

FIG. 7

FIG.8

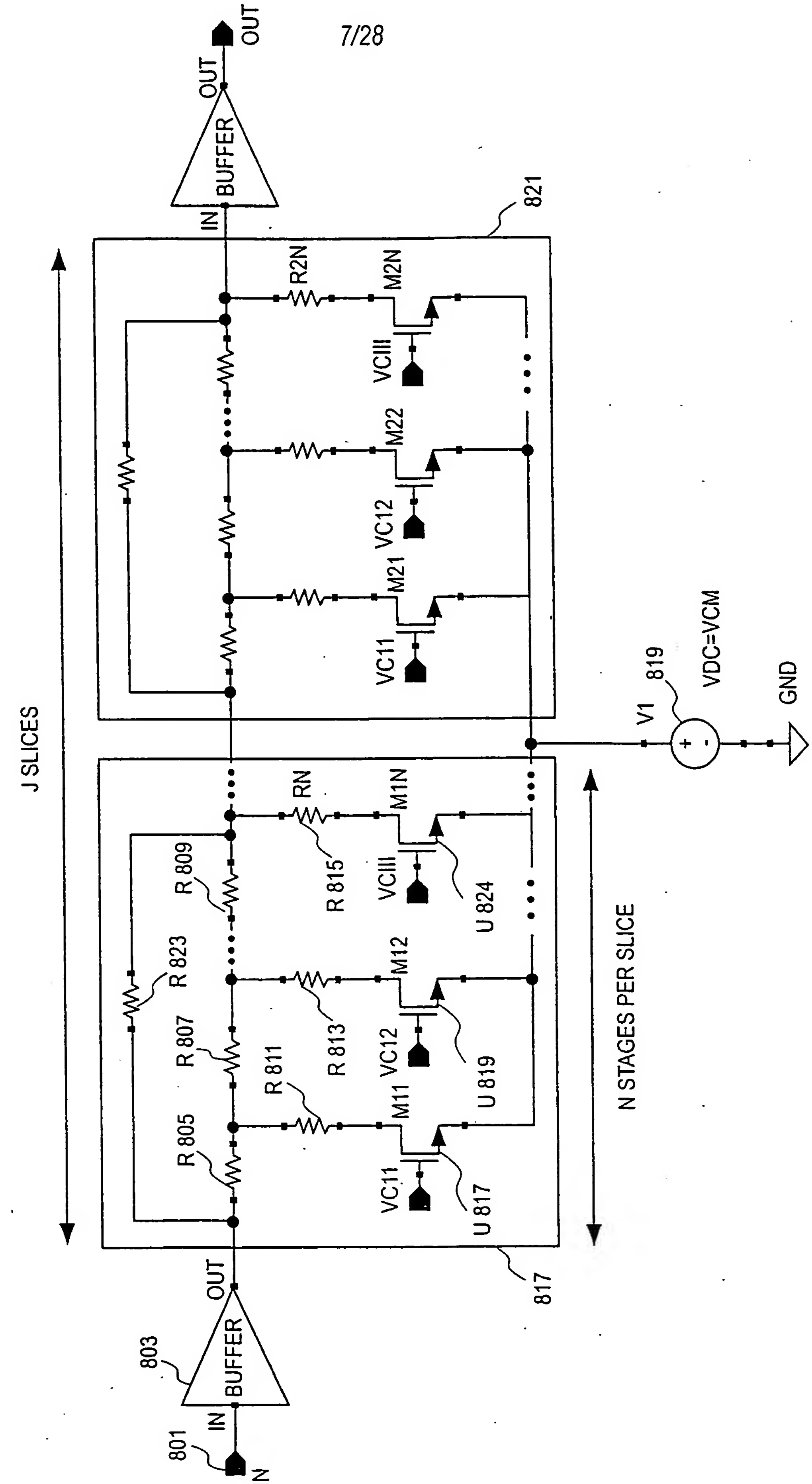

IN
801
IN
BUFFER
803
OUT
J SLICES
R 805
R 807
R 809
R 823
R 811
R 813
R 815
RN
M11
M12
M1N
VC11
VC12
VCIII
U 817
U 819
U 824
817
N STAGES PER SLICE
V1
819
VDC=VCM
GND
R2N
M21
M22
M2N
821
IN
BUFFER
OUT
OUT

FIG. 9
PRIOR ART

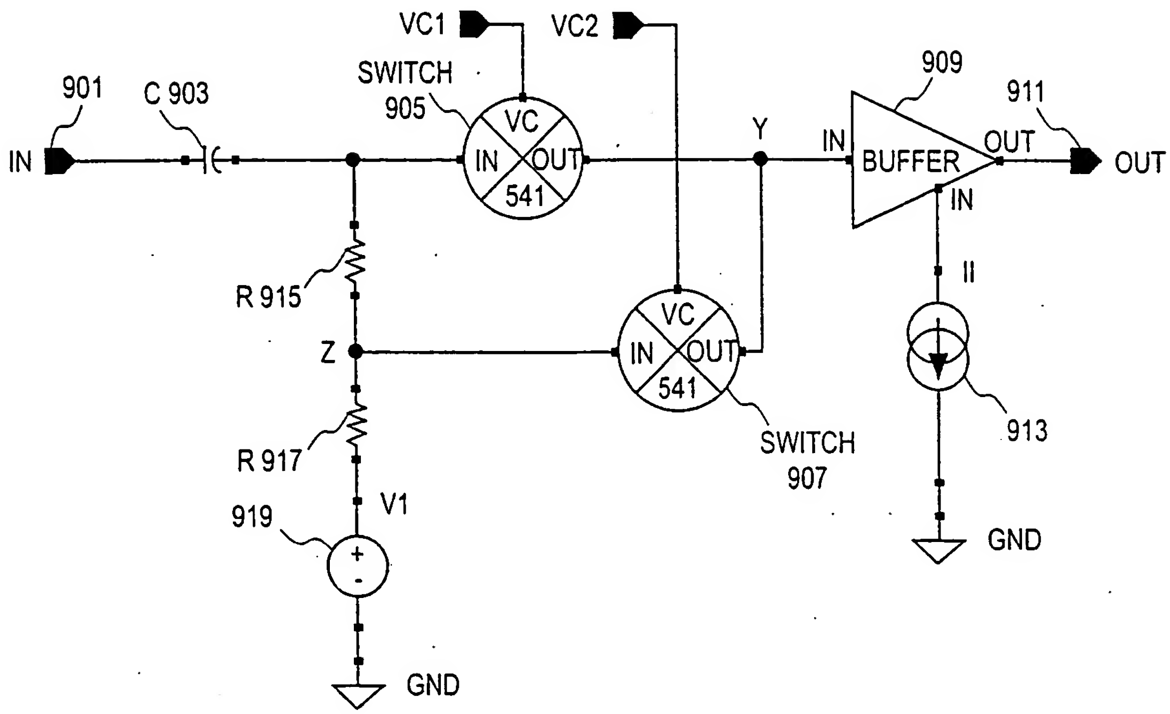


FIG.10
PRIOR ART

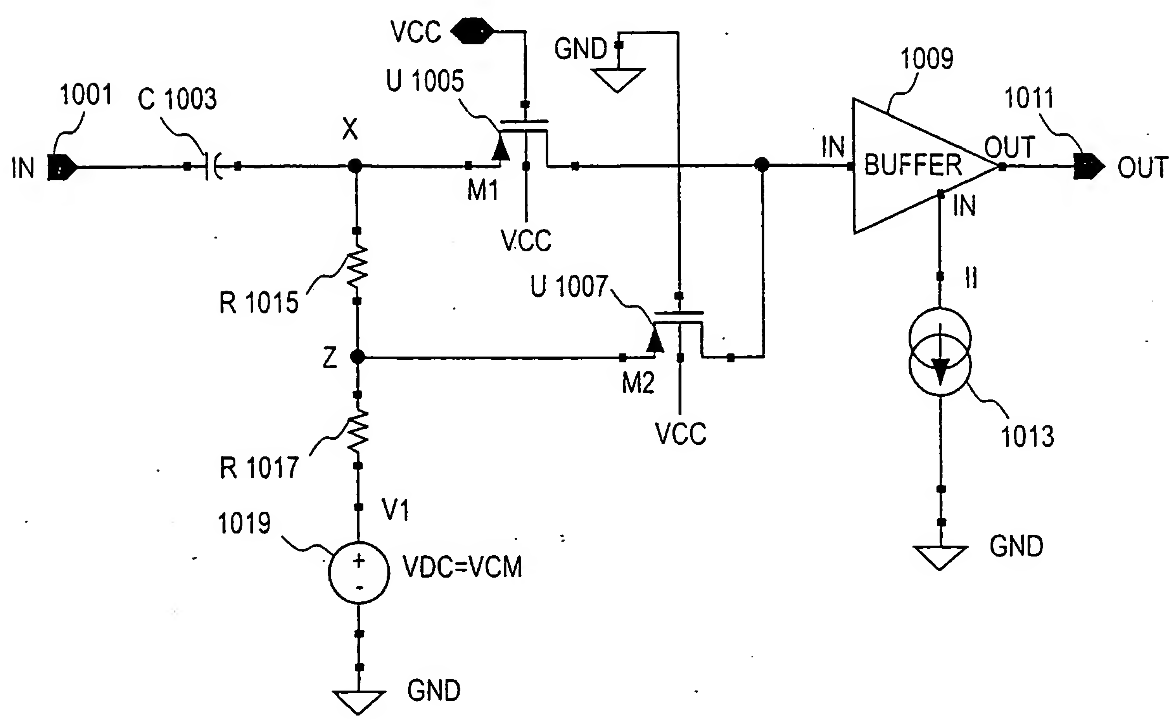


FIG. 11

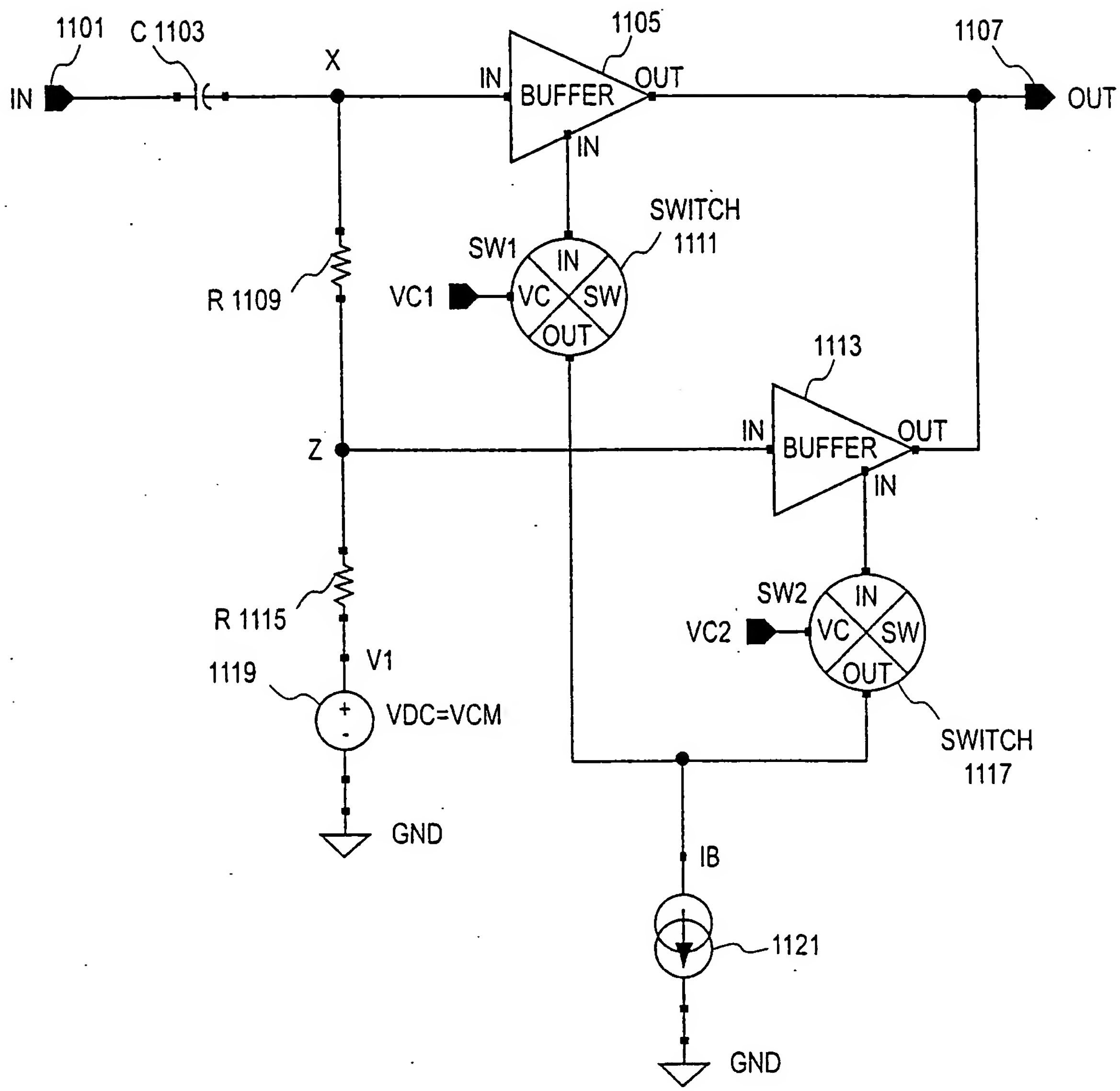

1101
C 1103
IN
X
IN
BUFFER
OUT
1105
IN
1107
OUT
SWITCH
1111
SW1
IN
VC1
VC
SW
OUT
R 1109
1113
IN
BUFFER
OUT
Z
IN
SW2
IN
VC2
VC
SW
OUT
SWITCH
1117
R 1115
V1
1119
VDC=VCM
GND
IB
1121
GND

FIG. 12

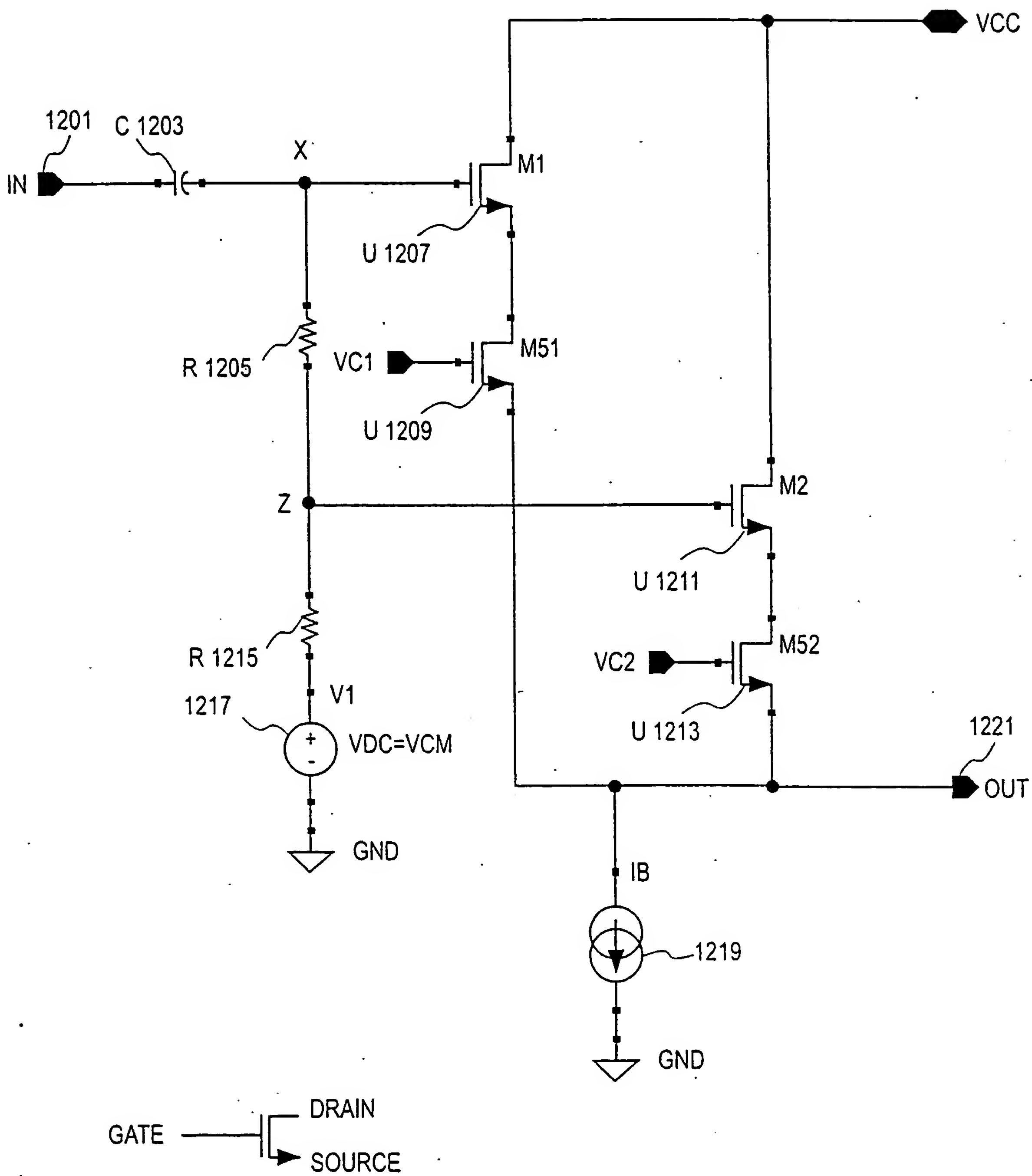
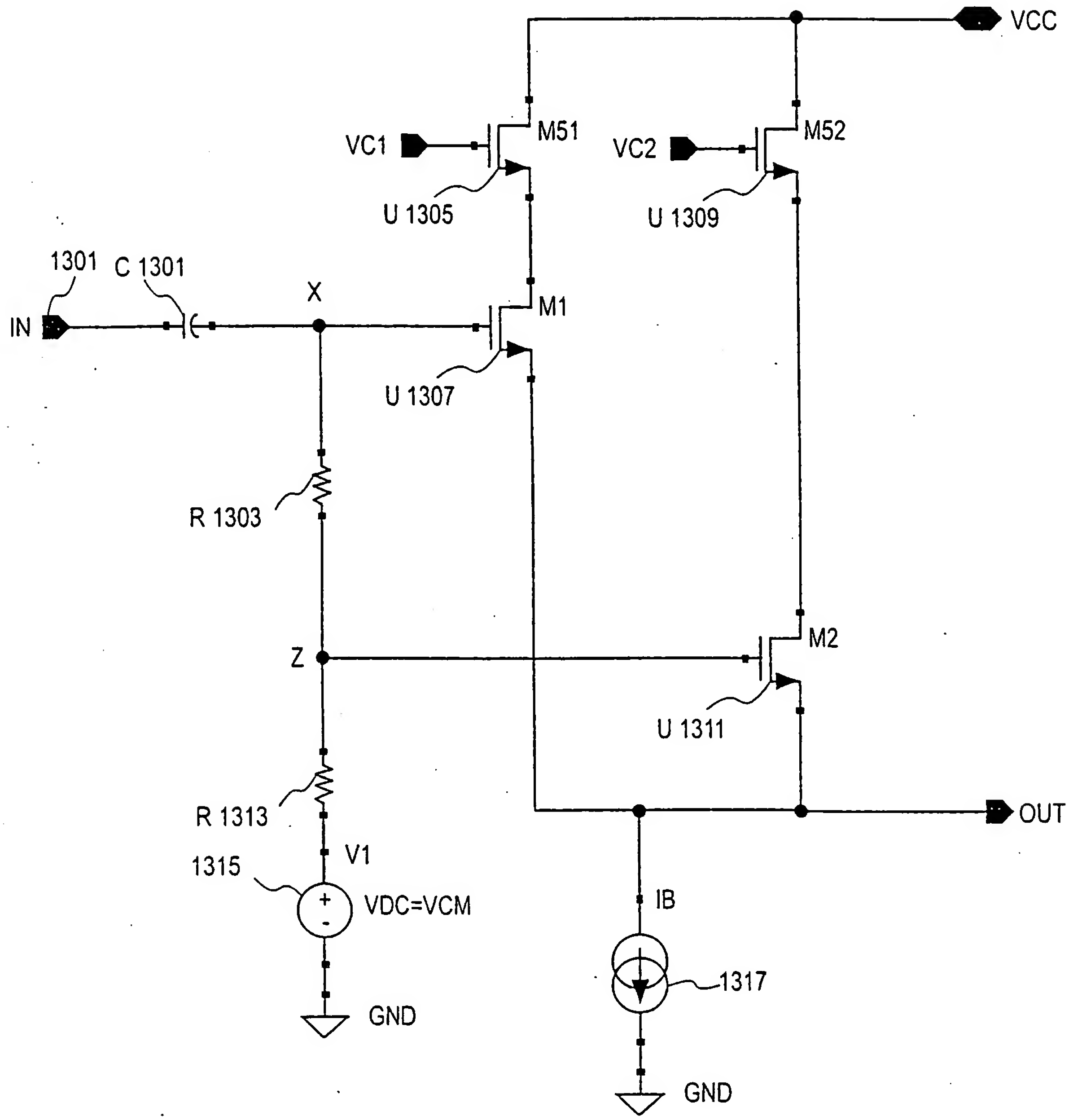

VCC
1201
C 1203
X
IN
M1
U 1207
R 1205
VC1
M51
U 1209
Z
M2
U 1211
R 1215
VC2
M52
V1
1217
U 1213
1221
VDC=VCM
OUT
GND
IB
1219
GND
DRAIN
GATE
SOURCE

FIG. 13


VCC
VC1
M51
VC2
M52
U 1305
U 1309
1301
C 1301
X
IN
M1
U 1307
R 1303
M2
Z
U 1311
R 1313
OUT
V1
1315
VDC=VCM
IB
1317
GND
GND

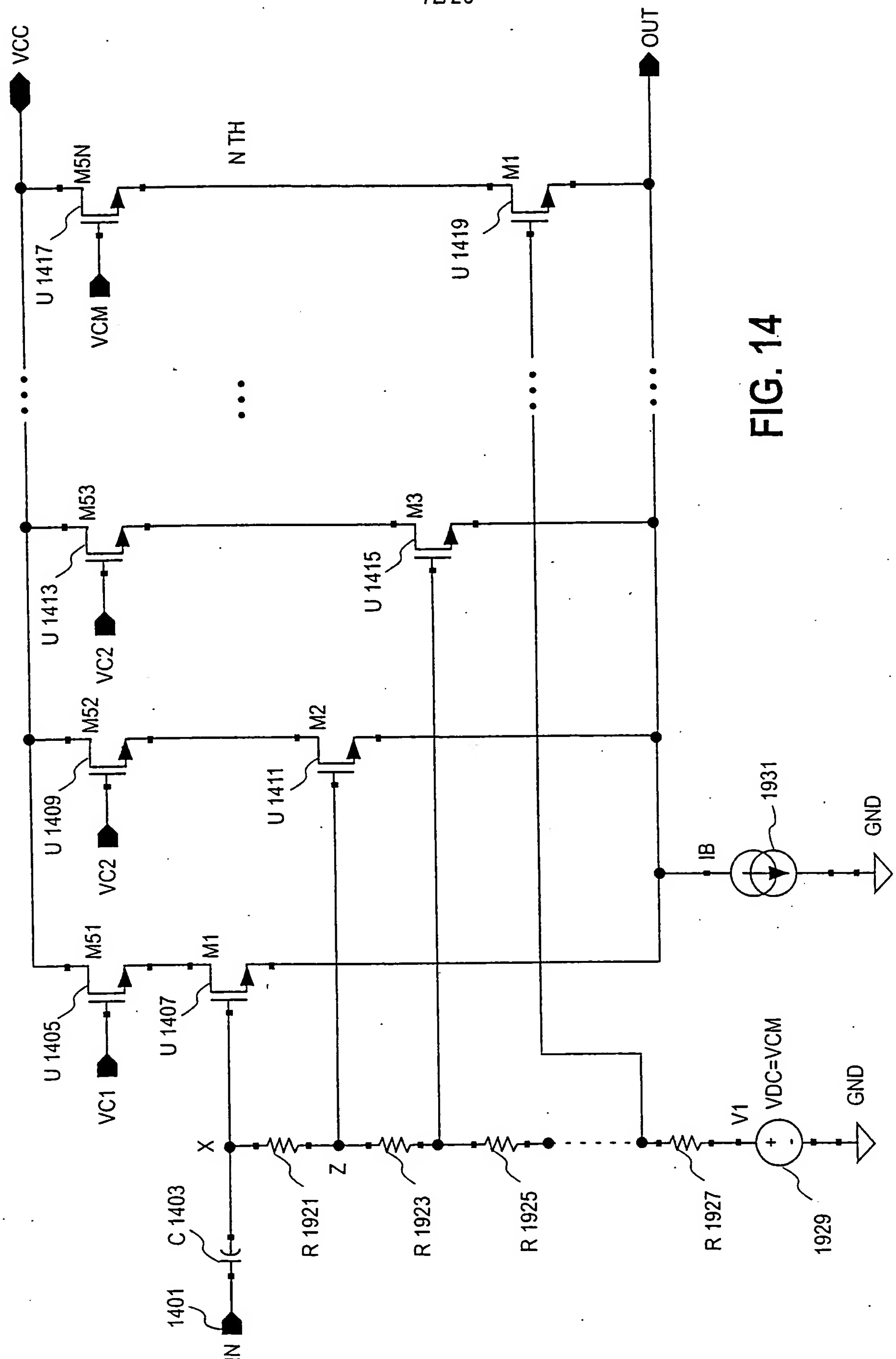

VCC
OUT
N TH
M5N
M1
U 1417
U 1419
VCM
M53
M3
U 1413
U 1415
VC2
M52
M2
U 1409
U 1411
VC2
IB
1931
GND
M51
M1
U 1405
U 1407
VC1
X
Z
C 1403
1401
IN
R 1921
R 1923
R 1925
R 1927
V1
VDC=VCM
GND
1929

FIG. 14

FIG. 15

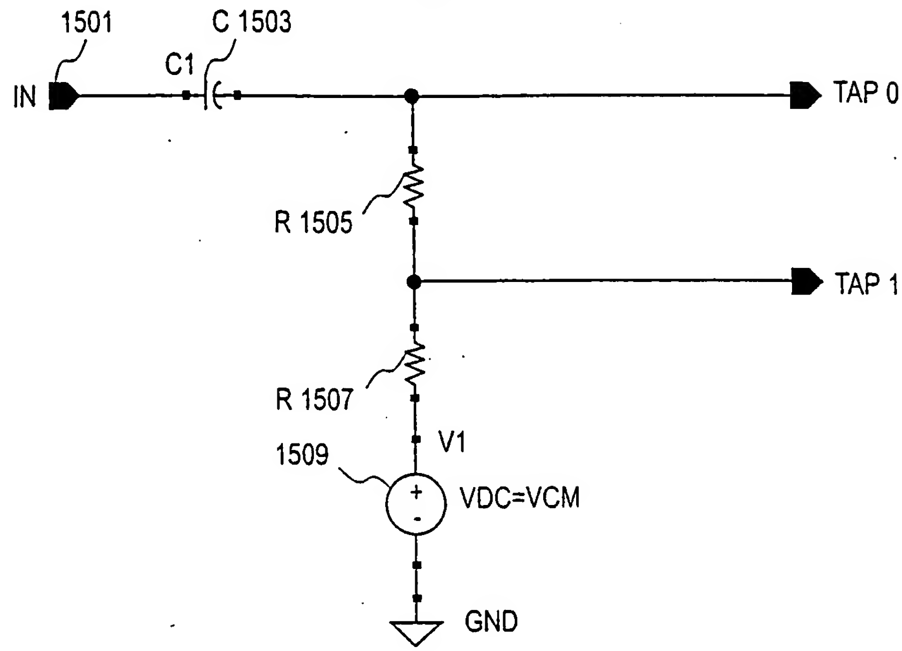

1501
C 1503
C1
IN
TAP 0
R 1505
TAP 1
R 1507
V1
1509
VDC=VCM
GND

FIG. 16

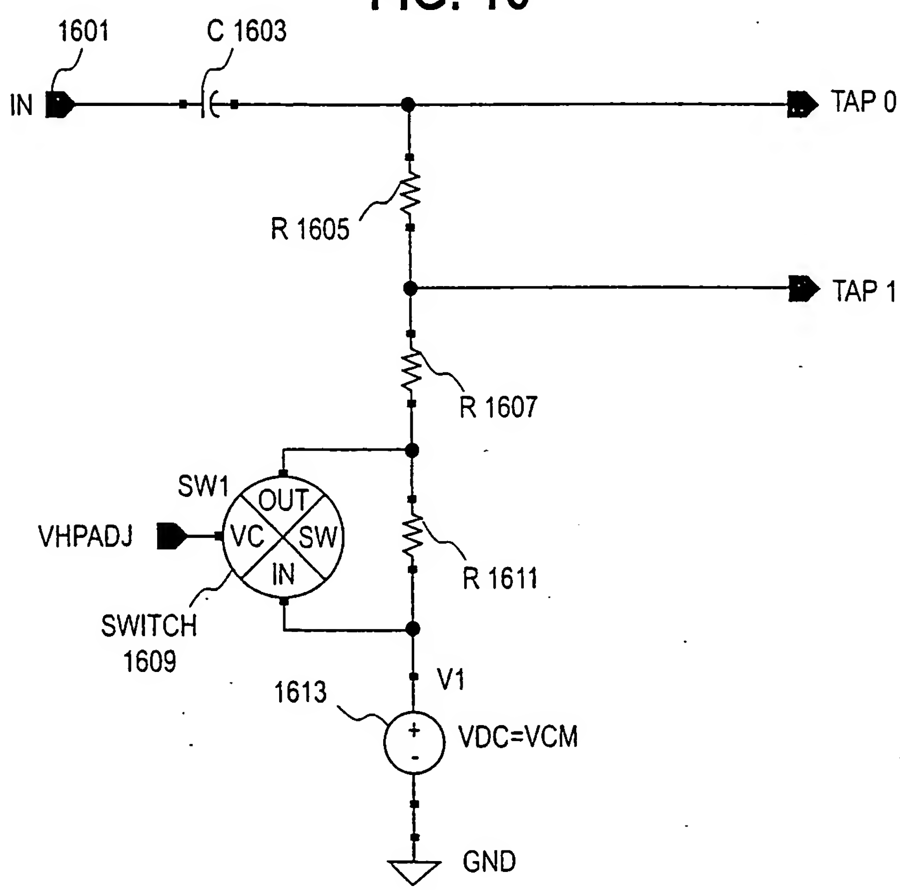

1601
C 1603
IN
TAP 0
R 1605
TAP 1
R 1607
SW1
OUT
VHPADJ
VC
SW
IN
SWITCH
1609
R 1611
V1
1613
VDC=VCM
GND

FIG. 17

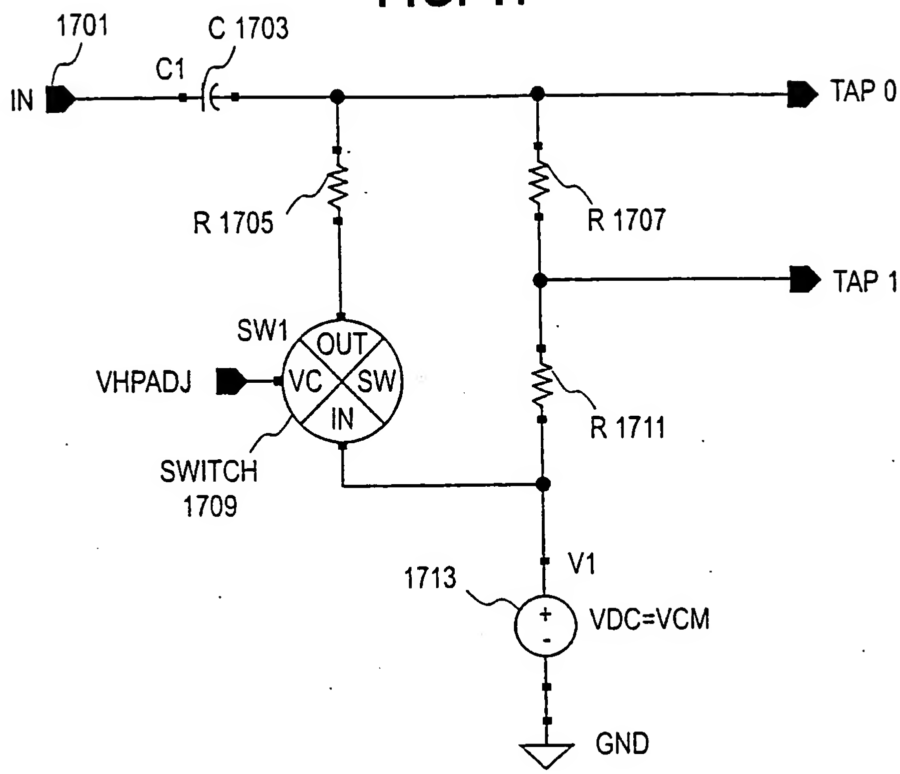

1701
C 1703
C1
IN
TAP 0
R 1705
R 1707
TAP 1
SW1
OUT
VHPADJ
VC
SW
IN
R 1711
SWITCH
1709
V1
1713
VDC=VCM
GND

FIG. 18

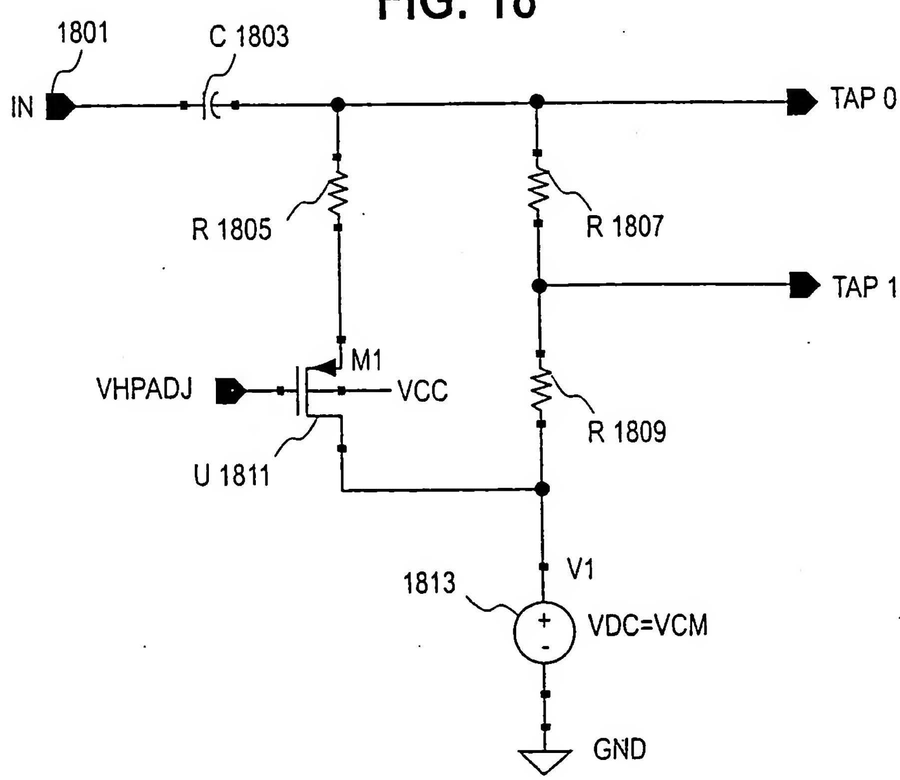
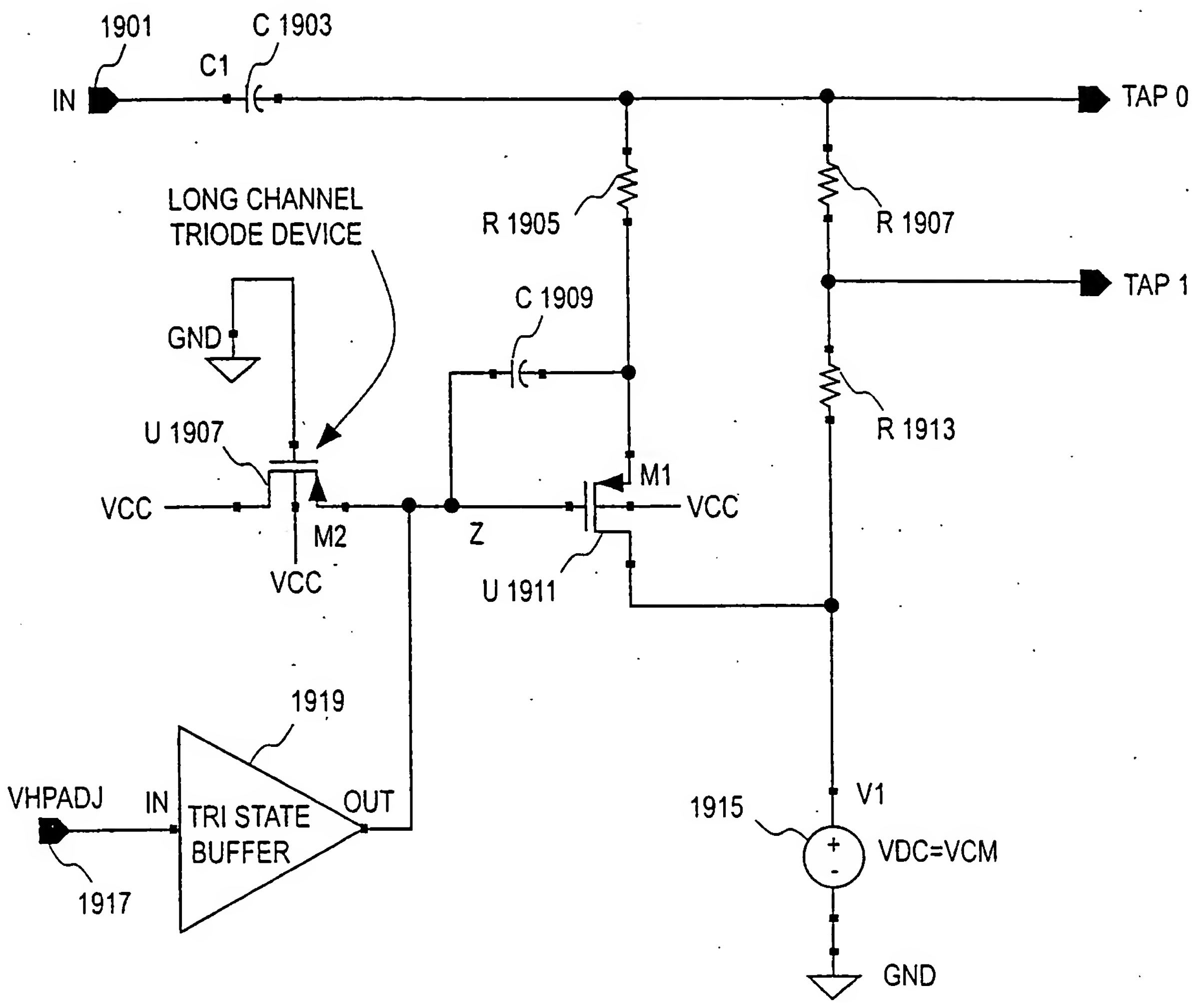

1801
C 1803
IN
TAP 0
R 1805
R 1807
TAP 1
M1
VHPADJ
VCC
R 1809
U 1811
V1
1813
VDC=VCM
GND

FIG. 19


1901
C 1903
C1
IN
TAP 0
LONG CHANNEL
TRIODE DEVICE
R 1905
R 1907
TAP 1
C 1909
GND
U 1907
R 1913
M1
VCC
VCC
M2
Z
VCC
U 1911
1919
VHPADJ
IN
TRI STATE
BUFFER
OUT
1917
1915
V1
VDC=VCM
GND

TITLE: GIGABIT ETHERNET TRANSCEIVER WITH
ANALOG FRONT END
INVENTOR: BEHZAD
APPLICATION NO.: UNASSIGNED,
CONF. NO. ; DOCKET NO. 13432US07
ATTORNEY: JAW, PHONE: 312-775-8000

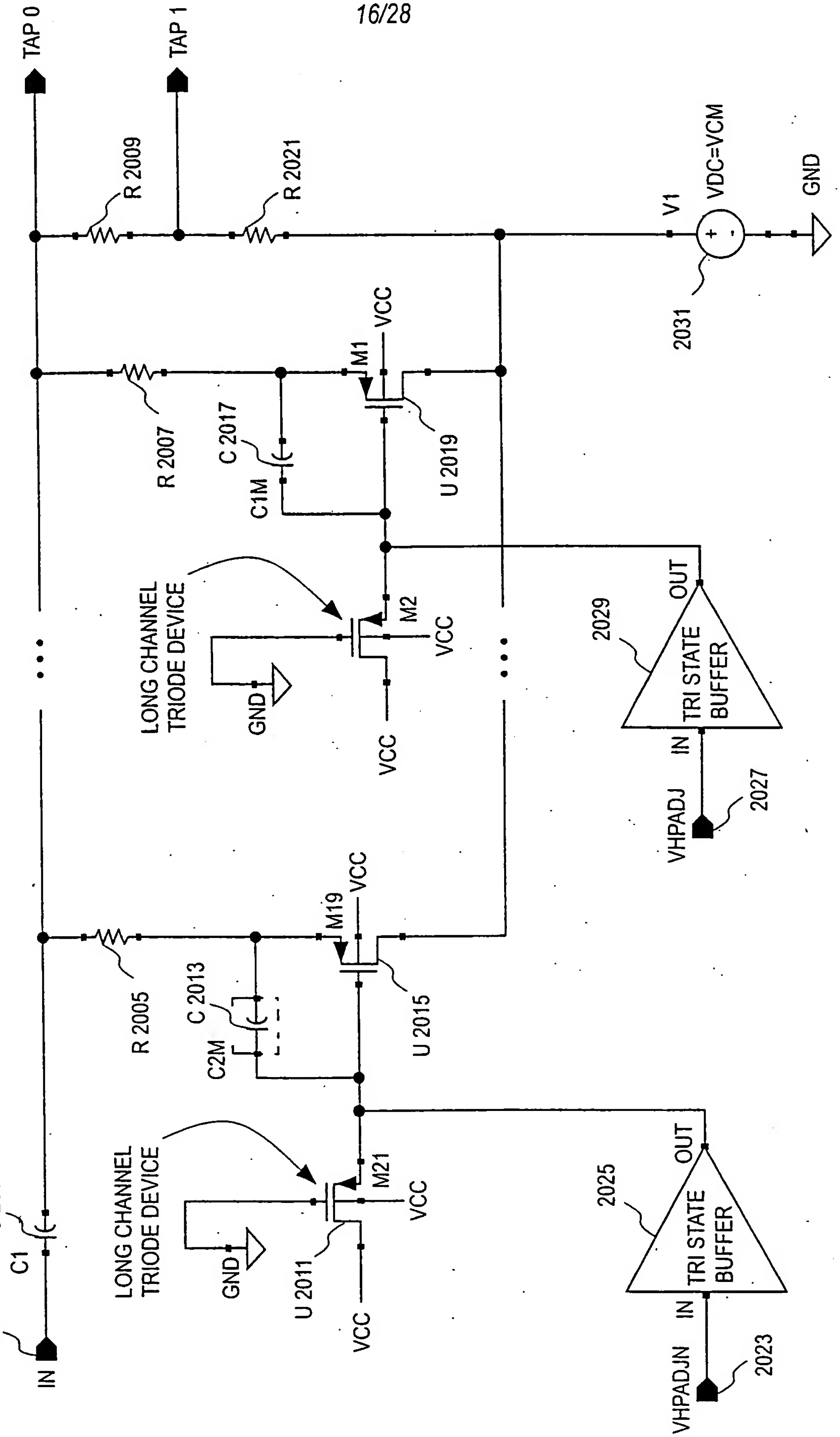


FIG. 20

TITLE: GIGABIT ETHERNET TRANSCEIVER WITH ANALOG FRONT END
INVENTOR: BEHZAD
APPLICATION NO.: UNASSIGNED,
CONF. NO. ; DOCKET NO. 13432US07
ATTORNEY: JAW, PHONE: 312-775-8000

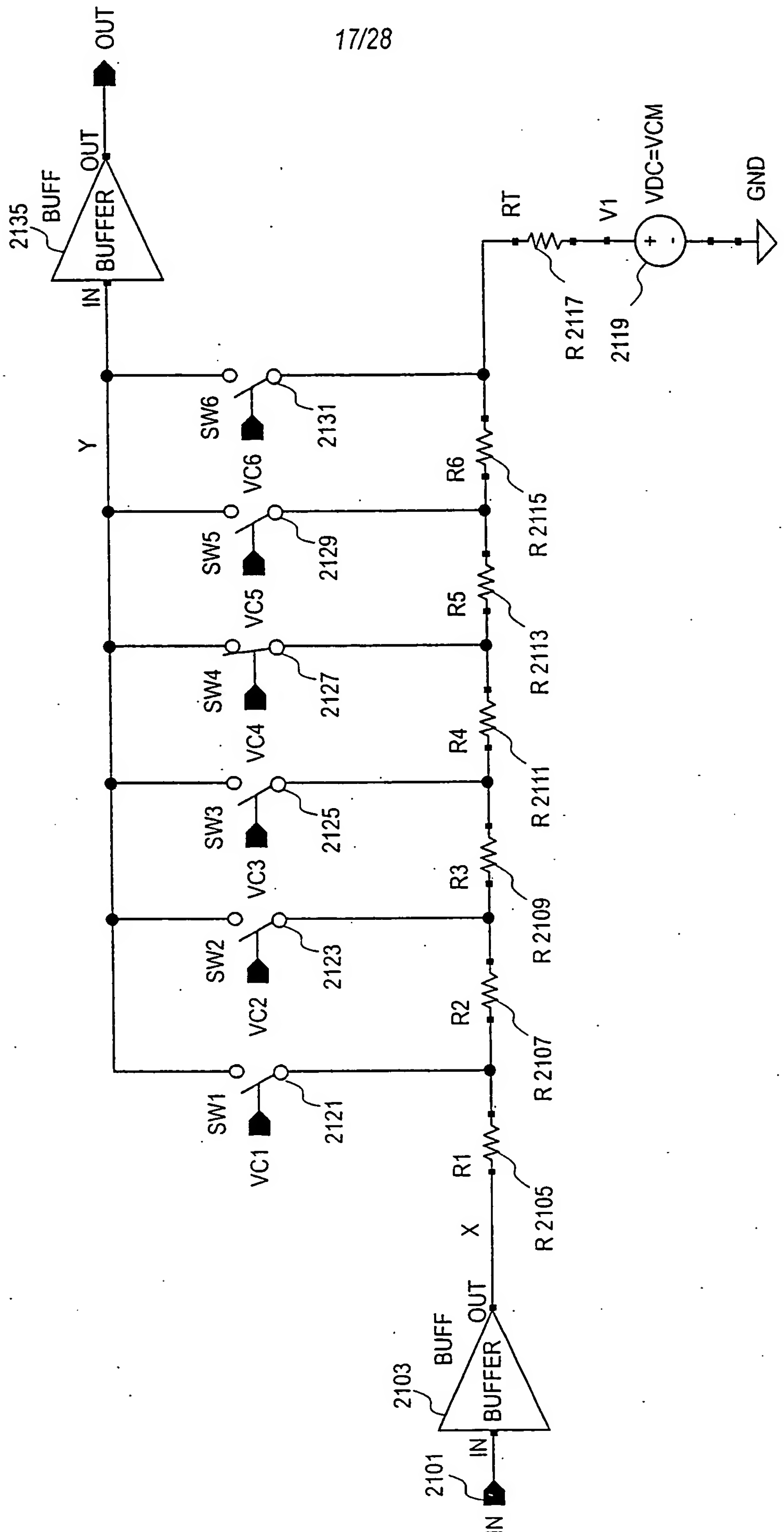


FIG. 21
PRIOR ART

TITLE: GIGABIT ETHERNET TRANSCEIVER WITH
ANALOG FRONT END
INVENTOR: BEHZAD
APPLICATION NO.: UNASSIGNED,
CONF. NO. ; DOCKET NO. 13432US07
ATTORNEY: JAW, PHONE: 312-775-8000

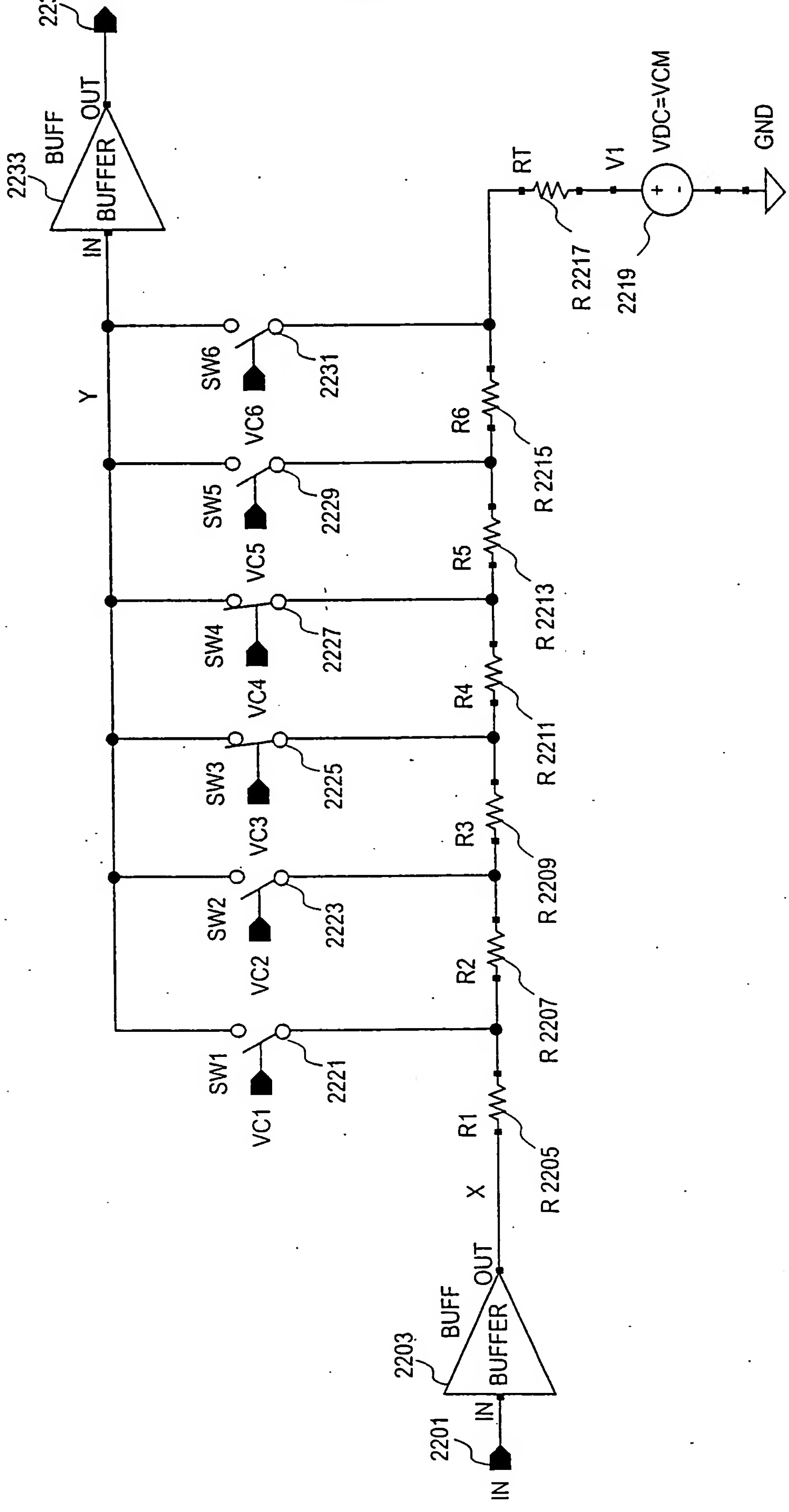
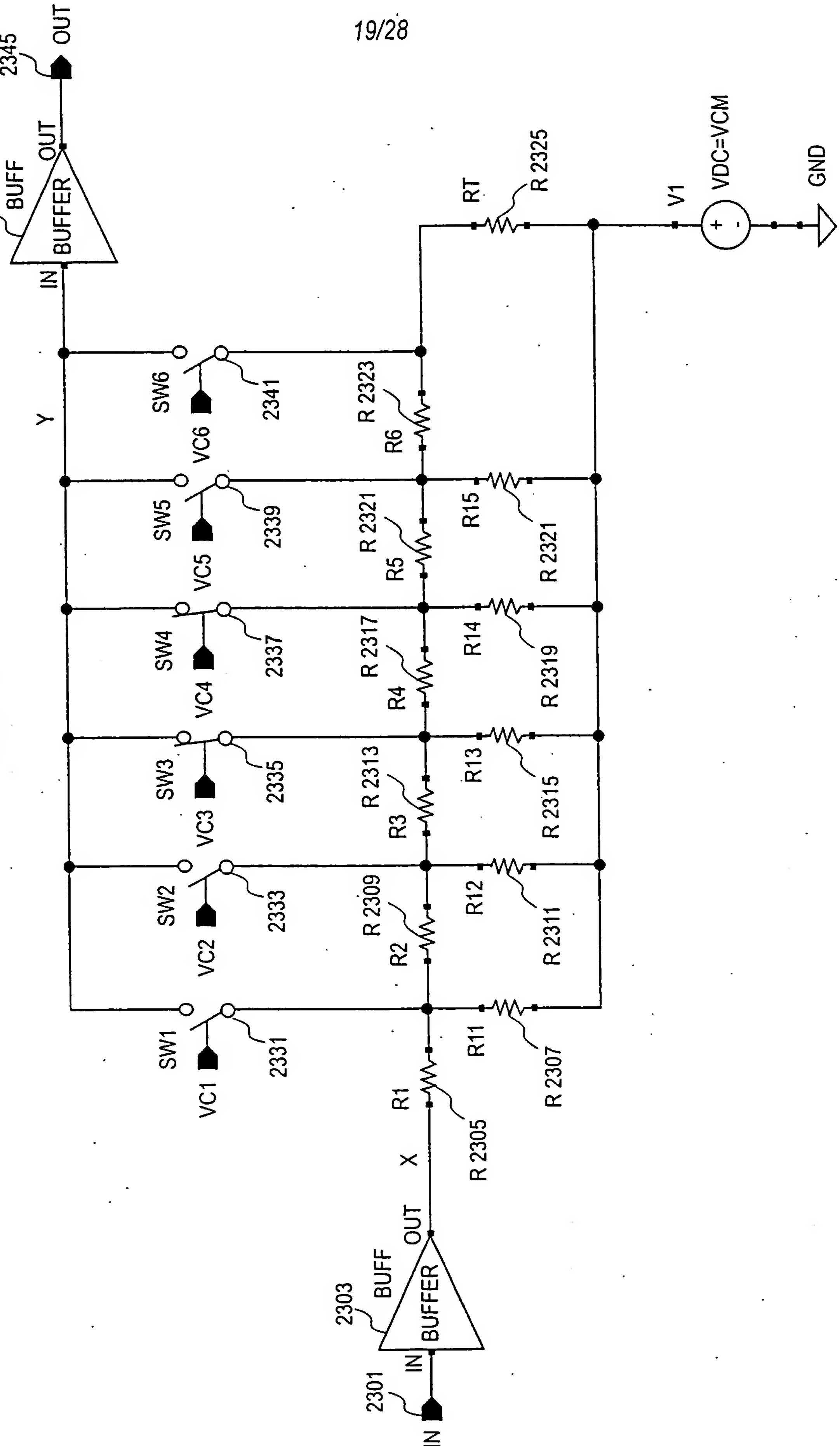


FIG. 22

TITLE: GIGABIT ETHERNET TRANSCEIVER
WITH ANALOG FRONT END
INVENTOR: BEHZAD
APPLICATION NO.: UNASSIGNED,
CONF. NO. ; DOCKET NO. 13432US07
ATTORNEY: JAW, PHONE: 312-775-8000

FIG. 23



TITLE: GIGABIT ETHERNET TRANSCEIVER
WITH ANALOG FRONT END
INVENTOR: BEHZAD
APPLICATION NO.: UNASSIGNED,
CONF. NO. ; DOCKET NO. 13432US07
ATTORNEY: JAW, PHONE: 312-775-8000

FIG. 24

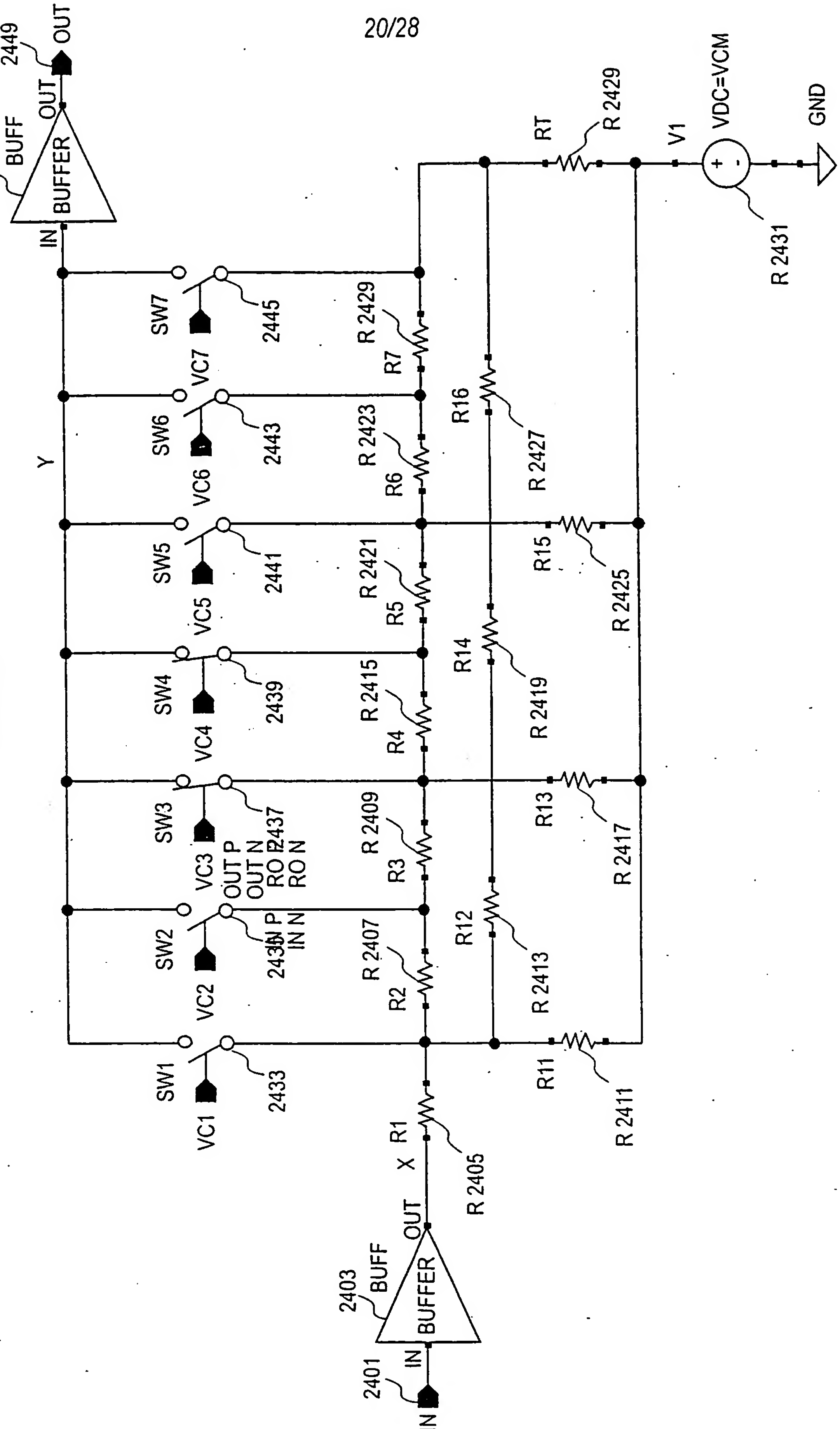


FIG. 25

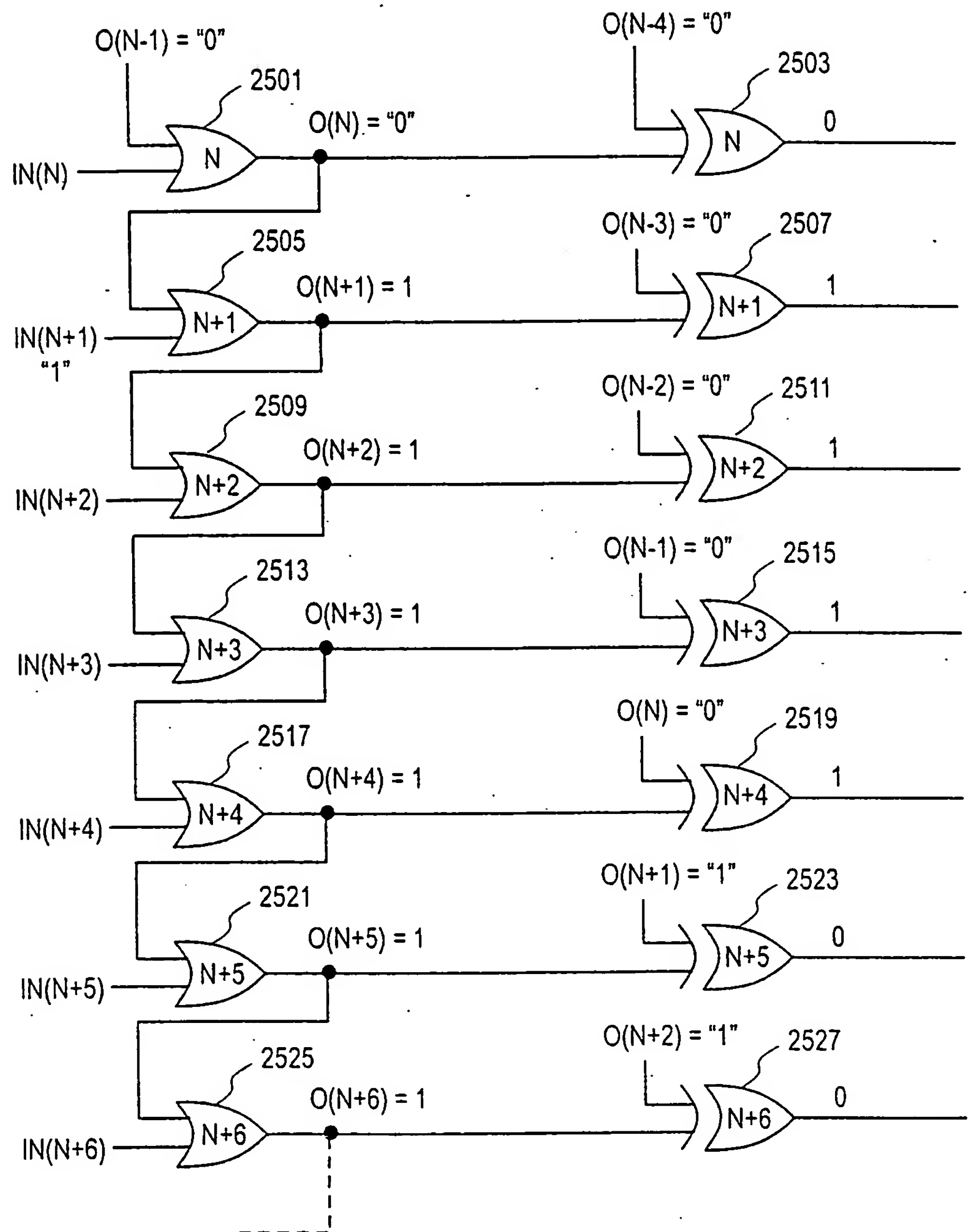

O(N-1) = "0"
2501
N
IN(N)
O(N) = "0"
O(N-4) = "0"
2503
N
0
2505
N+1
IN(N+1)
"1"
O(N+1) = 1
O(N-3) = "0"
2507
N+1
1
2509
N+2
IN(N+2)
O(N+2) = 1
O(N-2) = "0"
2511
N+2
1
2513
N+3
IN(N+3)
O(N+3) = 1
O(N-1) = "0"
2515
N+3
1
2517
N+4
IN(N+4)
O(N+4) = 1
O(N) = "0"
2519
N+4
1
2521
N+5
IN(N+5)
O(N+5) = 1
O(N+1) = "1"
2523
N+5
0
2525
N+6
IN(N+6)
O(N+6) = 1
O(N+2) = "1"
2527
N+6
0

FIG. 26

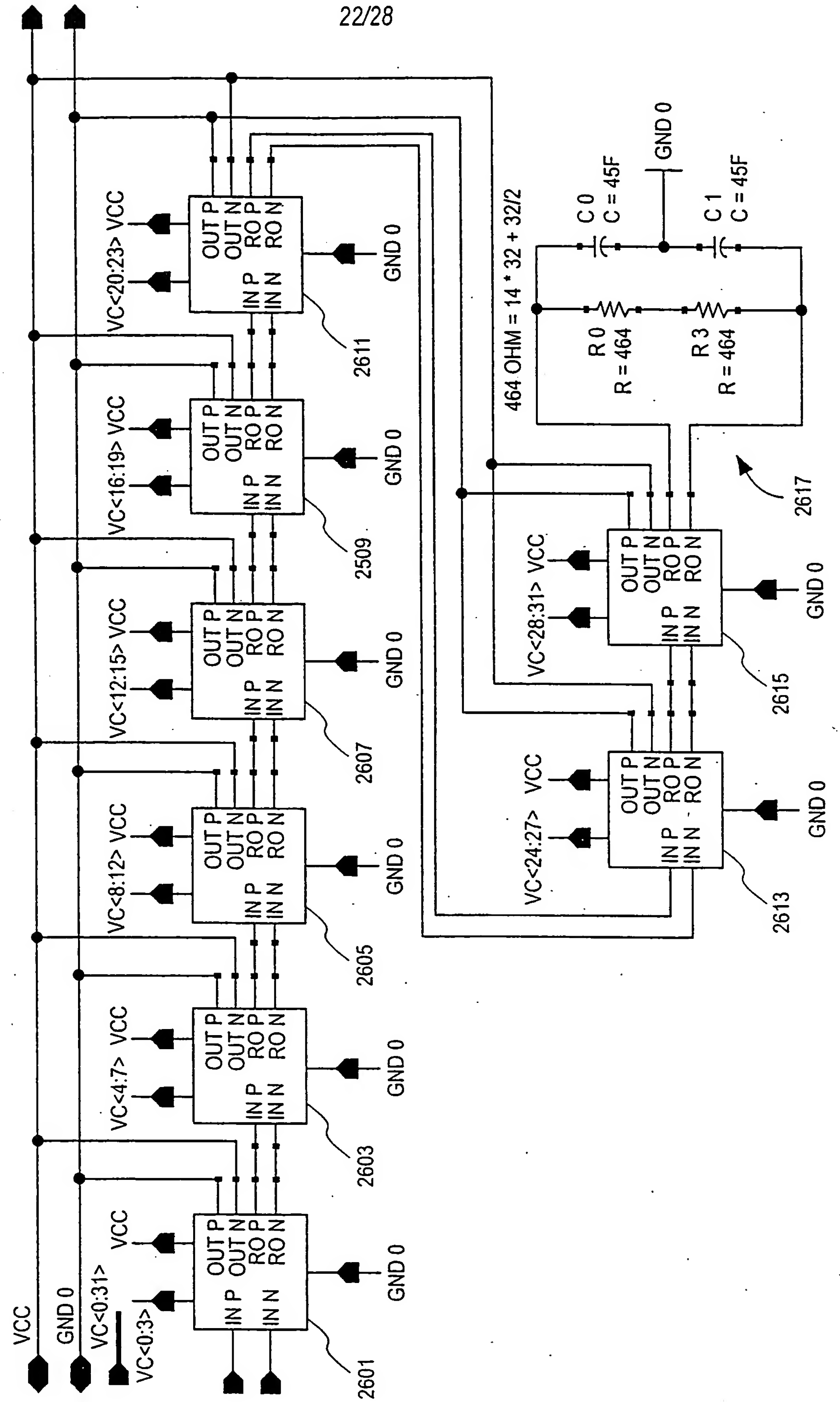

VCC
GND 0
VC<0:31>
VC<0:3>
VC<4:7> VCC
VC<8:12> VCC
VC<12:15> VCC
VC<16:19> VCC
VC<20:23> VCC
VC<24:27> VCC
VC<28:31> VCC
IN P
IN N
OUT P
OUT N
RO P
RO N
GND 0
2601
2603
2605
2607
2509
2611
2613
2615
2617
464 OHM = 14 * 32 + 32/2
R 0
R = 464
R 3
R = 464
C 0
C = 45F
C 1
C = 45F

FIG. 27

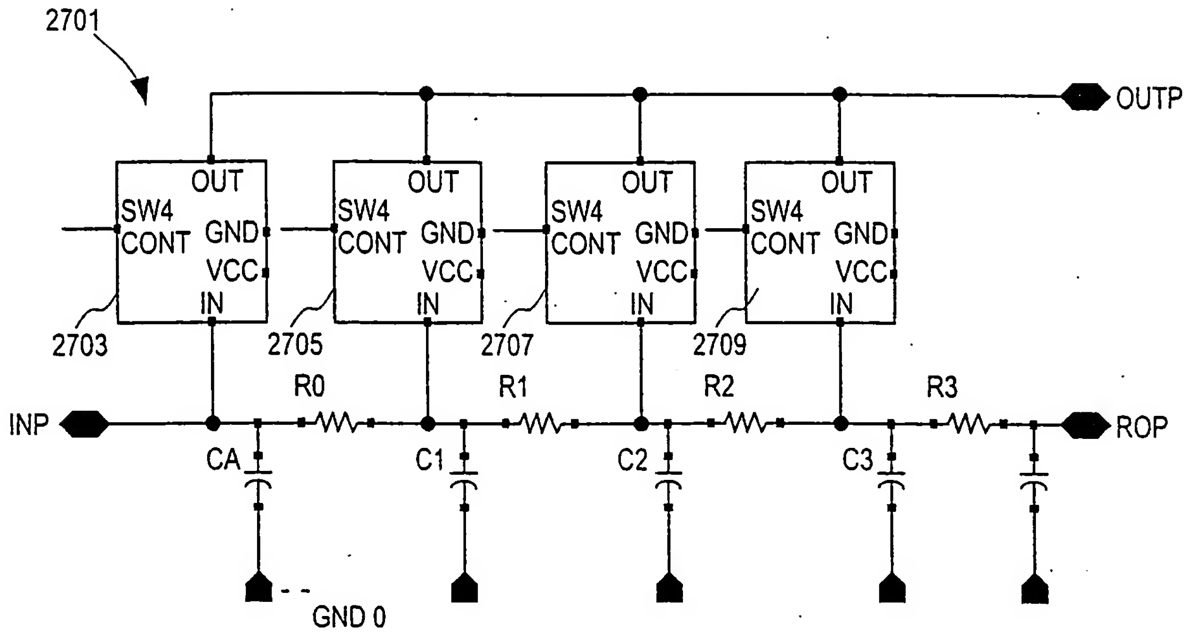
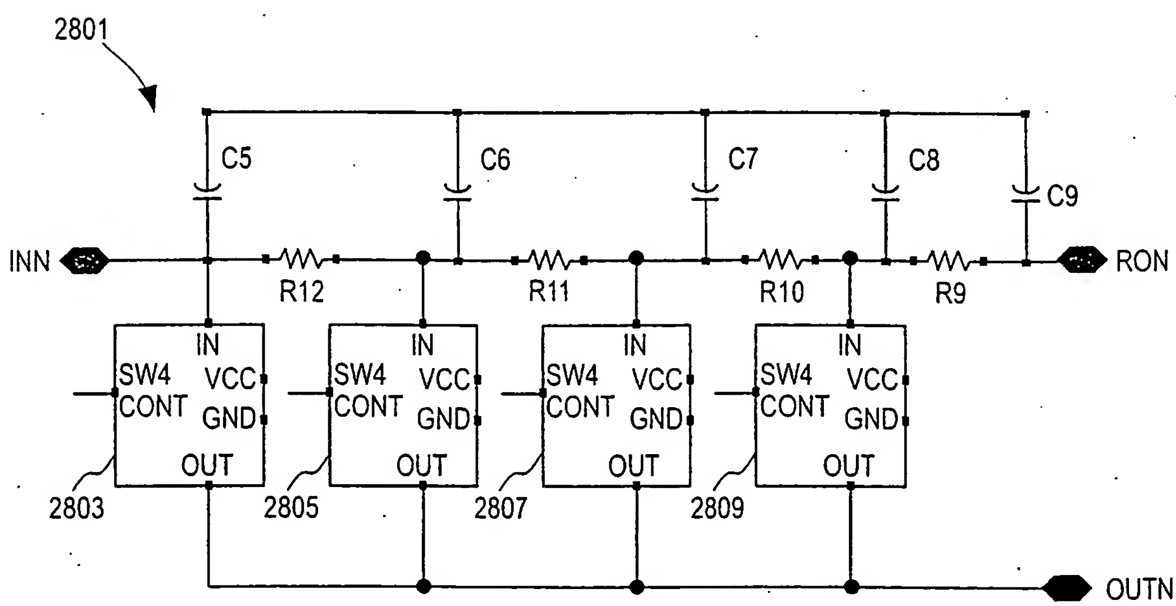

2701
OUTP
OUT
SW4
CONT
GND
VCC
IN
2703
2705
2707
2709
R0
R1
R2
R3
INP
ROP
CA
C1
C2
C3
GND 0

FIG. 28


2801
C5
C6
C7
C8
C9
INN
RON
R12
R11
R10
R9
IN
SW4
CONT
VCC
GND
OUT
2803
2805
2807
2809
OUTN

TITLE: GIGABIT ETHERNET TRANSCEIVER
WITH ANALOG FRONT END
INVENTOR: BEHZAD
APPLICATION NO.: UNASSIGNED,
CONF. NO. ; DOCKET NO. 13432US07
ATTORNEY: JAW, PHONE: 312-775-8000

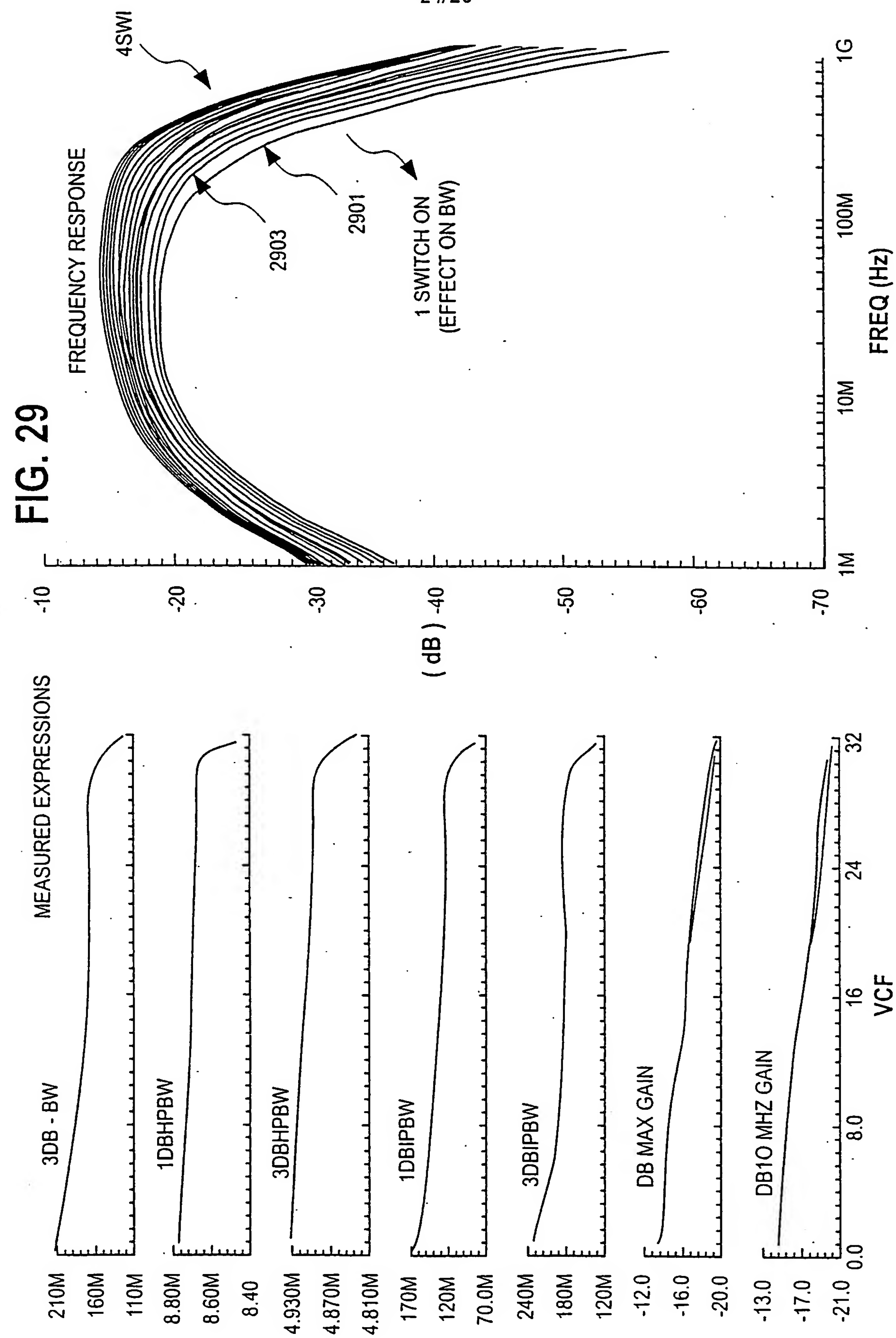


FIG. 29

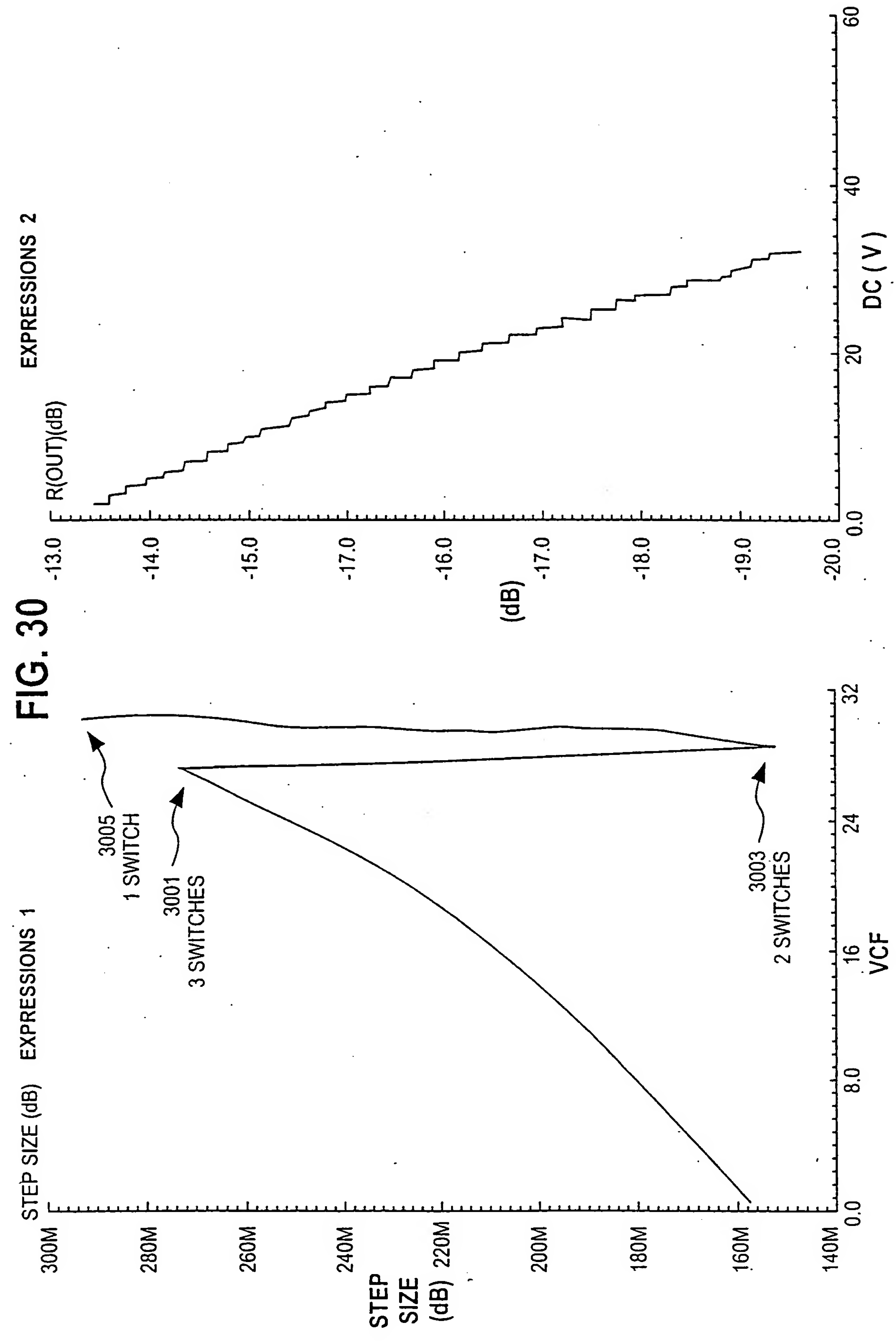

EXPRESSIONS 2
R(OUT)(dB)
-13.0
-14.0
-15.0
-17.0
-16.0
-17.0
-18.0
-19.0
-20.0
(dB)
0.0
20
40
60
DC (V)
STEP SIZE (dB)
EXPRESSIONS 1
300M
280M
260M
240M
220M
200M
180M
160M
140M
STEP SIZE (dB)
0.0
8.0
16
24
32
VCF
3005
1 SWITCH
3001
3 SWITCHES
3003
2 SWITCHES

FIG. 30

FIG. 31

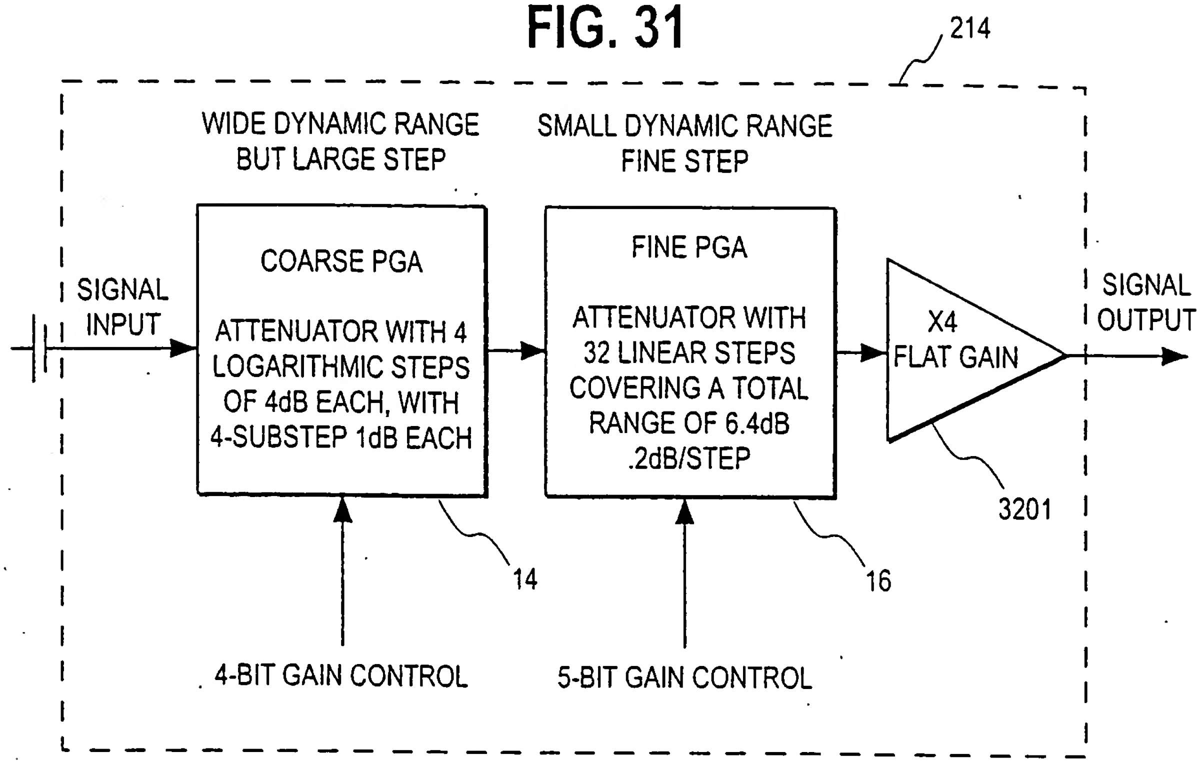
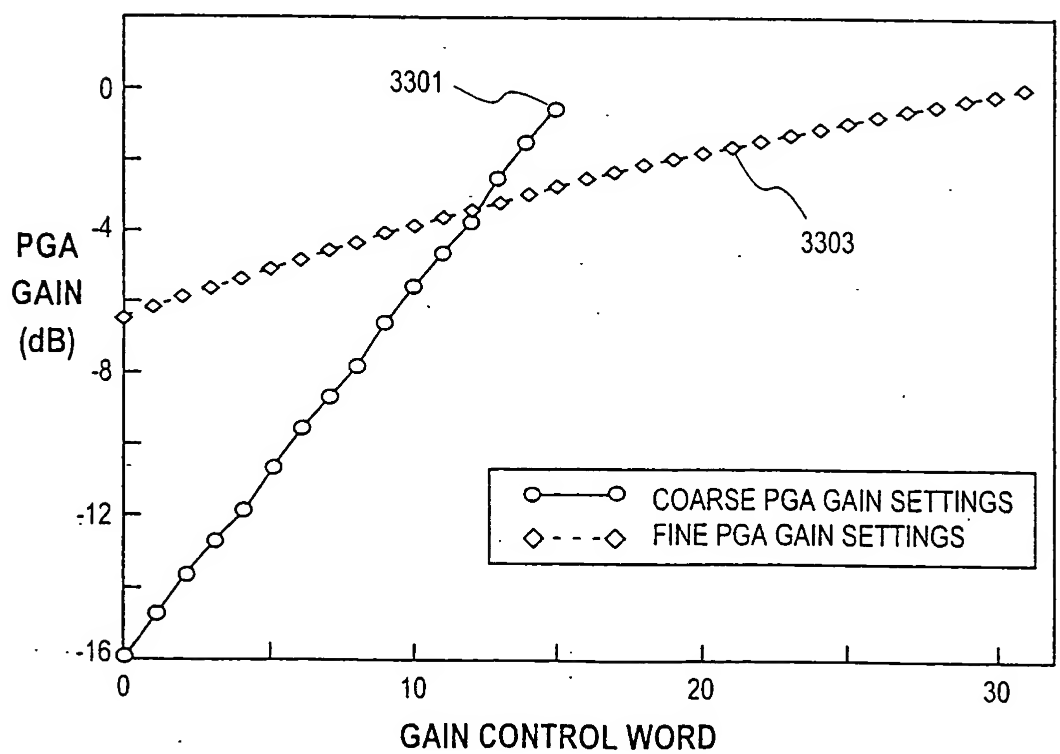
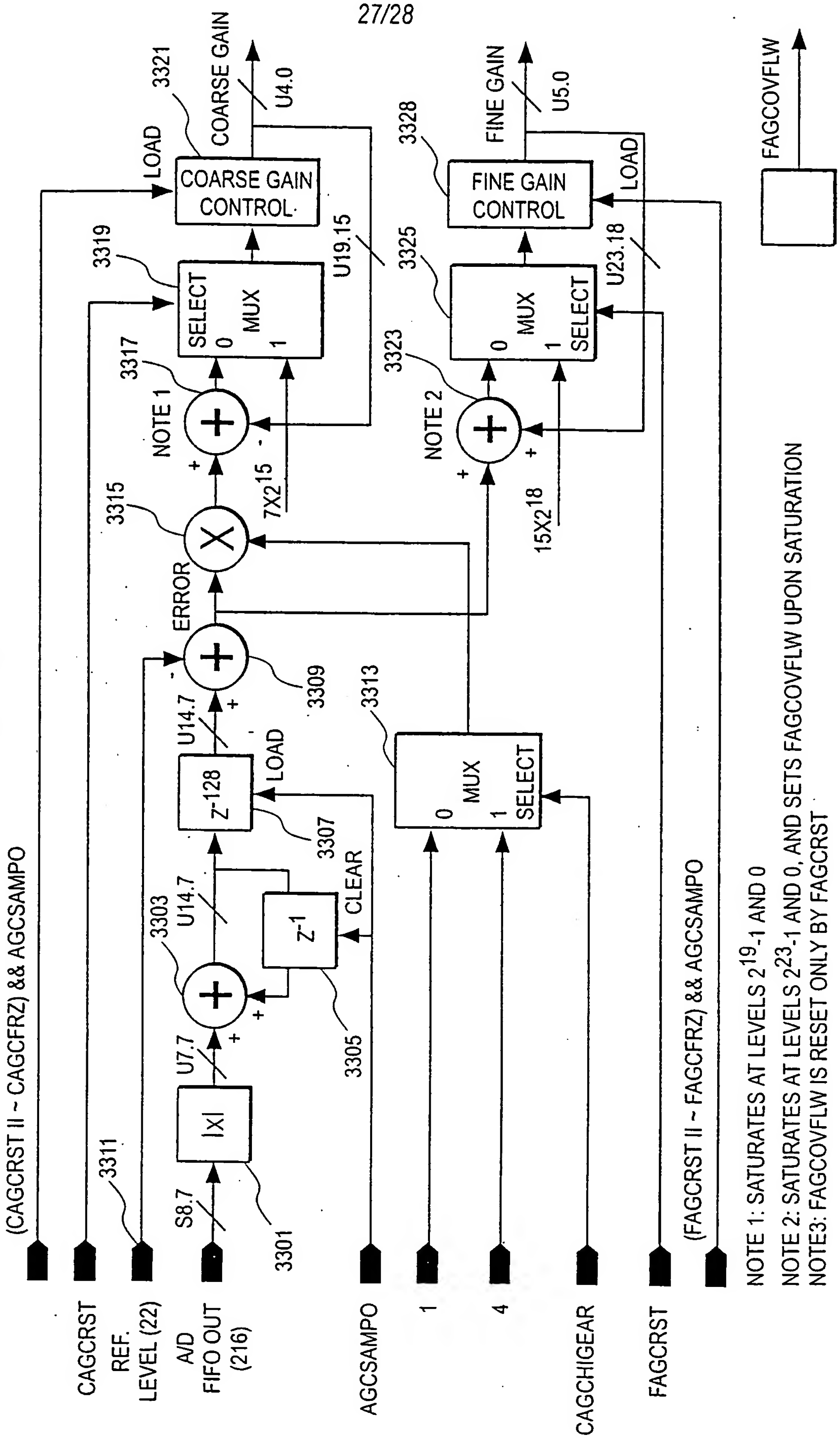

214
WIDE DYNAMIC RANGE
BUT LARGE STEP
SMALL DYNAMIC RANGE
FINE STEP
SIGNAL
INPUT
COARSE PGA
ATTENUATOR WITH 4
LOGARITHMIC STEPS
OF 4dB EACH, WITH
4-SUBSTEP 1dB EACH
FINE PGA
ATTENUATOR WITH
32 LINEAR STEPS
COVERING A TOTAL
RANGE OF 6.4dB
.2dB/STEP
X4
FLAT GAIN
SIGNAL
OUTPUT
3201
14
16
4-BIT GAIN CONTROL
5-BIT GAIN CONTROL

FIG. 32


PGA
GAIN
(dB)
0
-4
-8
-12
-16
3301
3303
COARSE PGA GAIN SETTINGS
FINE PGA GAIN SETTINGS
0
10
20
30
GAIN CONTROL WORD

TITLE: GIGABIT ETHERNET TRANSCEIVER
WITH ANALOG FRONT END
INVENTOR: BEHZAD
APPLICATION NO.: UNASSIGNED,
CONF. NO. ; DOCKET NO. 13432US07
ATTORNEY: JAW, PHONE: 312-775-8000

FIG. 33



NOTE 1: SATURATES AT LEVELS 2^{19}-1 AND 0
NOTE 2: SATURATES AT LEVELS 2^{23}-1 AND 0, AND SETS FAGCOVFLW UPON SATURATION
NOTE3: FAGCOVFLW IS RESET ONLY BY FAGCRST

FIG. 34

CABLE LENGTH (m)	100 BASE-TX	GIGABIT, 100 OHM	GIGABIT, 85 OHM	GIGABIT, 115 OHM
0	3.691281	4.193192	4.193192	4.193192
20	3.806628	4.501316	4.362110	4.291369
40	3.877284	4.528136	4.457336	4.429949
60	3.894216	4.733644	4.695307	4.646305
80	4.055372	4.878569	4.847844	4.810019
100	4.225522	4.983545	4.991296	4.968900
120	4.357733	5.134131	5.194401	5.154263
140	4.556012	5.266919	5.380943	5.366309
160	4.764462	-	-	-

TARGET E{IXI} = A/D CLIPPING LEVEL X (E{IXI}/RMS)/(PEAK/RMS)
= 127 X 0.7979/5.2 = 20